XMC-CPU/T10
XMC/PMC 64-bit PowerPC™ T1022 Processor Board with FPGA

High-End CPU for Test and Application

- Freescale™ PowerPC QorIQ T1022, 1.2 GHz, 64-bit architecture, Double Precision Floating Point Unit, Ethernet, ECC-RAM
- Xilinx® FPGA Artix 7 (XC7A75T) for local applications
- RTC
- 2x GB-Ethernet, 1x USB 2.0 (Host)
- 62 I/Os at connector PMC-P14 configurable via FPGA as single ended (LVTTL) or 31 LVDS pairs

Health Features and Fallback Flash

- Local voltage and temperature monitoring
- Fail save firmware update by means of fallback Flash
- Watchdog
- Over temperature protection

Wide Range of Software Support

- OS-9, QNX®, VxWorks® and Linux® BSPs available
- Example source code for the FPGA included in the BSPs
- Universal boot loader: U-Boot
- EtherCAT® master available

Customization on Request

- QorIQ T1014 or T1024 or T1042 are applicable
- Additional connector P16 with (e.g.) 73 LVTTL or 34 LVDS I/Os
- MRAM (512 Kbyte)
- Console RS-232 via P14
- CAN (with IRIG-B timestamp) via P14
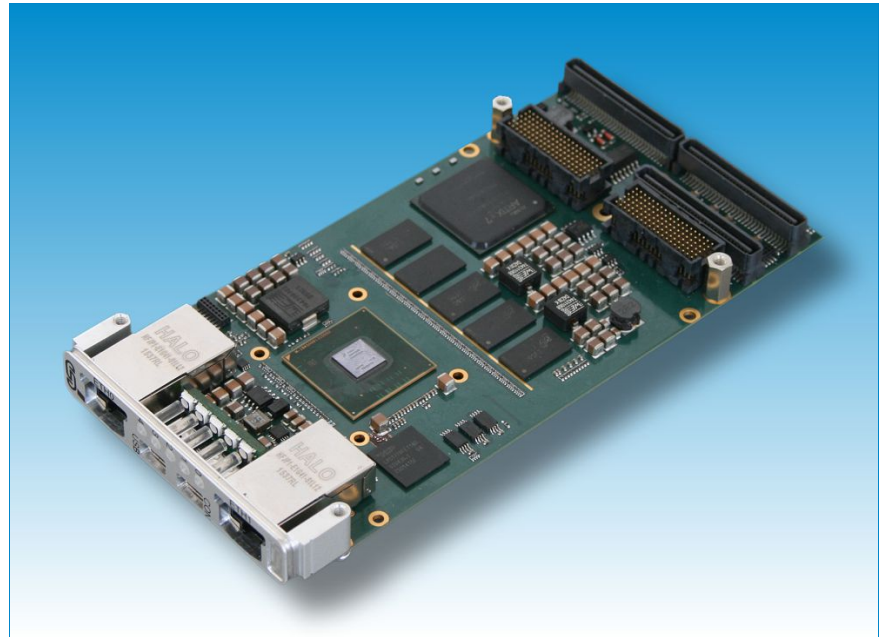
64-Bit XMC PowerPC Host CPU

The XMC-CPU/T10 is equipped with a PMC and an XMC interface.

The Freescale PowerPC QorIQ T1022 with 1.2 GHz features two 64-bit e5500 Power Architecture® processor cores with high-performance data path acceleration architecture (DPAA) and network peripheral interfaces.

The local memory bus is 64 bits wide plus 8 bits ECC with an overall capacity of 512 Mbyte. 16 Mbyte SPI Flash for boot loader and 32 Kbit I²C EEPROM for U-Boot environment offer non-volatile memory spaces.

The XMC-CPU/T10 is equipped with a second 16 Mbyte 'fallback' SPI Flash that is used for system recovery, if a system crash occurs during a firmware update.

FPGA for Local Applications

The Xilinx FPGA Artix 7 FPGA is connected to the CPU by local bus for low latency data exchange. For high bandwidth data exchange the FPGA is additionally connected via PCI Express to the CPU. 62 LVTTL-I/Os of the FPGA are routed to the PMC-P14 connector.

XMC/PMC Interfaces

The XMC interface comes with 4-lane PCIe bus and is designed according to VITA 42.3. The PMC interface supports 32 bit / 66 MHz PCI bus according to PCI Local Bus Specification 3.0.

Gigabit Ethernet

The XMC-CPU/T10 is equipped with two Gigabit Ethernet interfaces accessible at the front panel, which give an excellent base for EtherCAT® applications.

USB

The USB host port supports USB 2.0.

Software Support

The Flash memory carries the standard boot program U-Boot and enables the XMC-CPU/T10 to boot various operating systems from on-board Flash, network or USB. BSPs are available for OS-9, QNX, Linux and VxWorks. Example source code for the FPGA is included in the BSPs. The esd EtherCAT master is available and is implemented for VxWorks.

Customization on Request

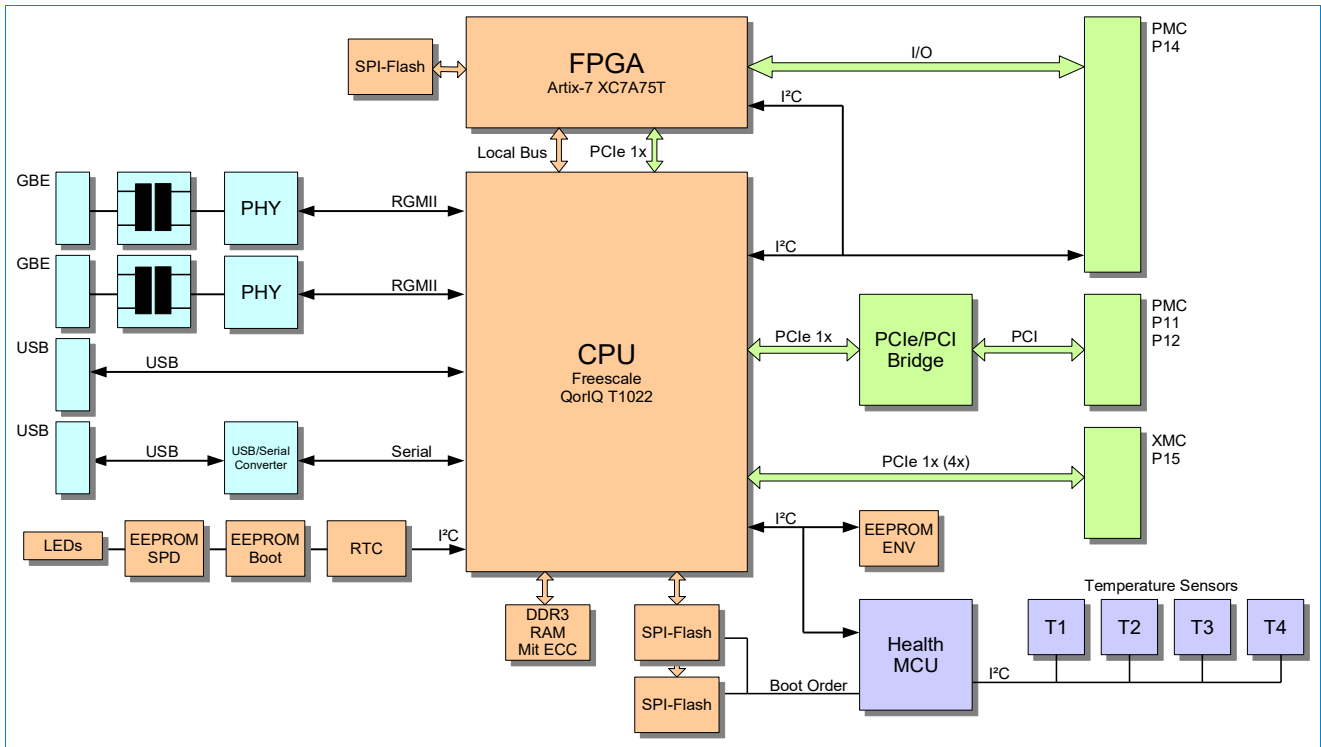A CAN IP-core (CAN esdACC) is available on request, implemented in a customized configuration (number of CAN nodes, routing FPGA ↔ P14). Additional 73 LVTTL I/Os at connector P16 or 34 LVDS I/Os are available. Other CPU-types (T1014, T1024, T1042) are applicable, also an additional MRAM and the Console (RS-232) via P14.

(This product is under development. It will be available Q4 2016.)

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Block Diagram labels:

SPI-Flash — FPGA (Artix-7 XC7A75T) — I/O — PMC P14

Local Bus — PCIe 1x — I²C

GBE — PHY — RGMII

GBE — PHY — RGMII

USB — USB

USB — USB — USB/Serial Converter — Serial

CPU Freescale QorIQ T1022

PCIe 1x — PCIe/PCI Bridge — PCI — PMC P11 P12

PCIe 1x (4x) — XMC P15

I²C — EEPROM ENV

LEDs — EEPROM SPD — EEPROM Boot — RTC — I²C

DDR3 RAM Mit ECC — SPI-Flash — SPI-Flash — Boot Order

Health MCU — I²C — Temperature Sensors: T1 T2 T3 T4

Technical Specifications:

Microcontroller and Memory:

Microcontroller	Freescale PowerPC™ QorIQ T1022, 64-bit, 1.2 GHz, Double Precision Floating Point Unit
Memory	512 Mbyte DDR3 RAM, 64 bits wide + 8 bit ECC, 32 Mbyte Flash for boot loader with health controller, 32 Kbit I²C EEPROM for U-Boot environment, 32 Kbit I²C EEPROM for Bootstrapping, 4 Kbit I²C EEPROM for SPD info DDR RAM
Real Time Clock	RTC with Gold Cap, backup time min. 7 days

Bus Interfaces

XMC	XMC according to VITA 42.3, 4-lane PCI EXPRESS® acc. to PCIe 1.1 (with T1022, T1042)
PMC	PMC according to IEEE Std 1386-2001, connectors: P11, P12, P14 PCI bus according to PCI Local Bus Specification 3.0, 32 bit 33/66 MHz, 3.3 V (5 V tolerant), PCI bus master capability
Voltage level	3.3 V (signal level), 5 V tolerant

Health:

Voltage monitor	For all internal voltages and temperatures
Temperature monitor	4x XMC power board I²C temperature sensors, CPU temperature sensor
Watchdog	CPU watchdog

Interfaces:

Ethernet	2x Gigabit Ethernet, 1000BaseT, IEEE802.3 at RJ45-connectors in front panel
USB host	USB 2.0 Full Speed (480 Mbit/s), Mini USB socket type AB in front panel
Console (serial)	1x Via bus powered USB device interface at Mini USB socket type-B in front panel

Interfaces (continued):

Digital I/O	62x single ended LVTTL-I/O (3.3V only) at PMC-P14 or (configurable via FPGA) 31 LVDS pairs (3.3V only) at PMC-P14
I²C	1x I²C at PMC-P14

General:

Cooling method	Convection cooling
Operating temperature	0 °C ... 55 °C ambient
Storage temperature	0 °C ... 55 °C ambient
Relative humidity	0% ... 90 % (non-condensing)
Power supply voltage	3.3 V, 5 V or 12 V from XMC, $P_{3.3V+5V}$ max. 15 W
Dimensions	149 mm x 74 mm x 10 mm

Order Information:

Hardware		Order No.
XMC-CPU/T10	XMC QorIQ T1022 PowerPC CPU Board, 1.2 GHz, 512 Mbyte RAM	V.2030.01

Accessories		
XMC-CPU-ADAPTER-BDI	Interface to connect the Abatron BDI3000	V.2029.02
XMC-CPU-ADAPTER-FPGA	Interface to connect the Tool XILINX ChipScope	V.2029.03
XMC-CPU-ADAPTER-NXP	Interface to connect NXP (Health controller)	V.2029.04

Software Support		
XMC-CPU/T10-OS9	OS-9 BSP	V.2030.56
XMC-CPU/T10-QNX	QNX BSP	V.2030.55
XMC-CPU/T10-Linux	Linux BSP	V.2030.57
XMC-CPU/T10-VxW	VxWorks BSP	V.2030.58
EtherCAT Master-VxW 6.x/PPC	Object code	P.4500.20