CPCI-CAN/400-4

4x CAN (CANopen®, J1939 or ARINC 825), IRIG-B, with Bus Master DMA

4 High-Speed CAN Interfaces for CompactPCI® with Bus Master DMA

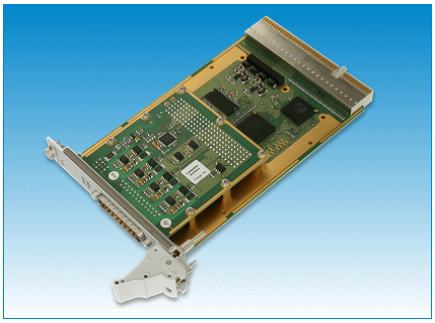
- *CAN interfaces according to ISO 11898-2 with electrical isolation*
- *Capable of 100% CAN bus load*
- *Reduces system load by bus master DMA transfer*
- *Enhanced diagnostic features e.g. CAN Error Injection*
- *33/66 MHz CompactPCI interface*

Realtime OS Drivers, J1939 and ARINC825 Higher Layer Protocol Support

- *Drivers and higher layer protocols for Windows®, Linux®, VxWorks®, QNX®, RTX, On Time RTOS-32 and others*
- *CANopen, J1939 and ARINC 825 protocol available*
- *CAN is driven by approved esd Advanced CAN Core (esdACC) CAN controller*

IRIG-B Input

- *IRIG-B input (expedient for ARINC 825 application)*



CPCI CAN Interface

The CPCI-CAN/400-4 is a CompactPCI board in 3U format, that features four High-Speed CAN interfaces according to ISO 11898-2. CAN is driven by the esd Advanced CAN Core (esdACC) CAN controller implemented in the Xilinx Spartan 3e FPGA. The CPCI-CAN/400-4 provides high resolution hardware timestamps.

IRIG-B

The CPCI-CAN/400-4 IRIG-B features an IRIG-B interface that offers inputs for analog or RS-422 IRIG-B coded signals. Both are electrically isolated. IRIG-B evaluation is controlled by an additional microcontroller. IRIG-B is used directly for CAN timestamping.

Software Support[1]

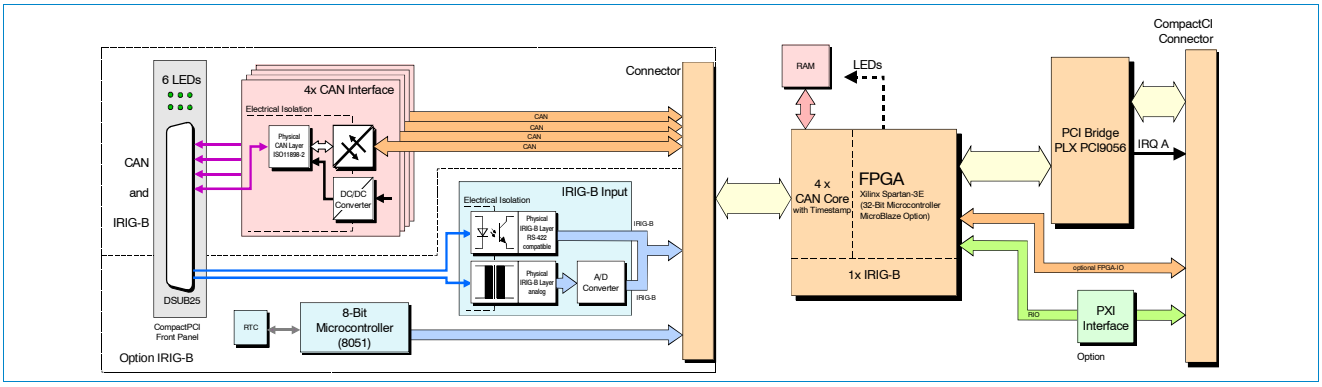
Operating system independent CAN layer 2 API (NTCAN).
Multiple Higher Level Protocols available

- *CANopen Master- and Slave-Stack*
- *J1939 (Windows only)*
- *ARINC825*

Options PXI and µC

The CPCI-CAN/400-4 optionally features a PXI interface:
The signals TRG 0-7, CLK 10 and STAR are controlled via the FPGA. The signals LBL/LBR1-12 are looped through.
An optional 32-bit MicroBlaze µC is available in the FPGA. Please, contact our sales team (sales@esd.eu) for further information.

(This product is in life cycle stage End of Life.)



Technical Specifications:

CompactPCI Interface and Microprocessor:	
Interface	*PCI bus according to PCI Local Bus Specification 2.2, 32 bit 33/66 MHz, 3.3 V (5 V tolerant), bus master DMA capability*
Memory	*BlockRAM: 72 KB, DRAM: 64 MB*

CAN:	
Interface	*4x CAN high-speed interface acc. to ISO11898-2, differential, electrically isolated, bit rate up to 1 Mbit/s*
CAN controller	*According to ISO 11898-1 (CAN 2.0 A/B)*

General:	
Ambient temp.	*0 °C ...+50 °C*
Rel. humidity	*Max. 90 %, non-condensing*
Connectors	*P1, P2, DSUB25 (male)*
Power supply	*5 V, I_{5V} = 265 mA (typical)* *3.3 V, $I_{3.3V}$ = 265 mA (typical)*
LEDs	*CAN status, 1x module status*

Order information:

Hardware		*Order No.*
CPCI-CAN/400-4 IRIG-B	*4x CAN, IRIG-B*	*C.2033.01*
CPCI-CAN/400-4	*4x CAN*	*C.2033.04*

CAN layer 2 drivers for Windows and Linux are included in delivery.

Software Support

Additional CAN layer 2 object licences including CD-ROM[1]*:*	
CAN-DRV-LCD QNX	*C.1101.32*
CAN-DRV-LCD VxWorks	*C.1101.55*
CAN-DRV-LCD RTX	*C.1101.35*
CAN-DRV-LCD OnTime-RTOS-32	*C.1101.45*
Higher layer protocols[1]*:*	
CANopen-LCD Windows/Linux	*C.1101.06*
CANopen-LCD QNX	*C.1101.17*
CANopen-LCD VxWorks	*C.1101.18*
CANopen-LCD RTX	*C.1101.16*
J1939stack for Windows	*C.1130.10*
J1939 stack for Linux	*C.1130.11*
ARINC825-LCD Windows / Linux	*C.1140.06*
ARINC825-LCD QNX	*C.1140.17*
ARINC825-LCD VxWorks	*C.1140.18*
ARINC825-LCD RTX	*C.1140.16*

[1] *For detailed information about the driver availability for your operating system please contact our sales team.*

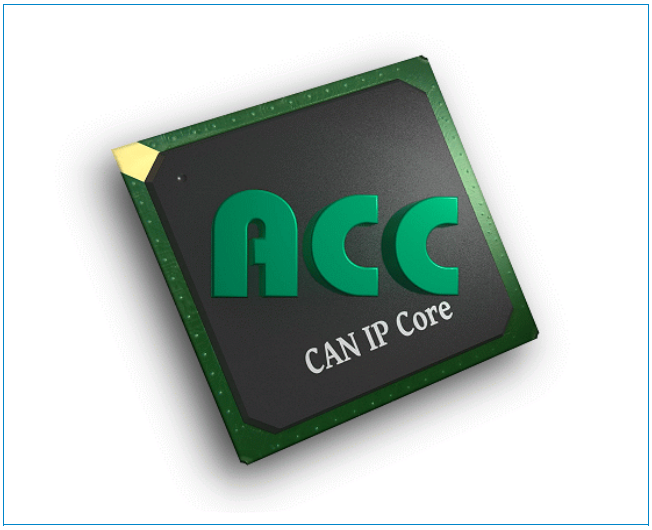
esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany
Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu

CPCI-CAN/400-4

esd CAN Module driven by Advanced CAN Core

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- 11-bit and 29-bit CAN IDs
- Bit rates from 10 kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)
- Busload measurement



Superior esdACC Features[1]:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- TX TS FIFO
  - 16 frames
  - High priority
  - 64 bit timestamp
  - Bit time accuracy for CAN transmission
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.

Superior esdACC Features[1] (continued):

- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)

[1] *Availability of the Superior esdACC Features depends on the operating system and the hardware. Please contact our sales team for further information.*

Driver Availability:

Windows, Linux[2], QNX[2], VxWorks[2], RTX[2]

[2] *For detailed information about the driver availability for your operating system and the particular esd CAN interface please contact our sales team.*

Available Higher Layer Protocol Libraries:

CANopen, ARINC825, J1939

For further information on the esdACC IP Core please contact our sales team.

esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
Email: info@esd.eu