PCI Express® Mini Card with 2 CAN or 2 CAN FD Interfaces

Single Lane PCIe Mini Card with Altera® FPGA for 2x CAN or 2x CAN FD
- 2 CAN (FD) interfaces according to ISO 11898-2
- Bus mastering and local data management by FPGA
- PCIe® Mini interface according to Mini Card Electromechanical Spec. R1.2
- Supports MSI (Message Signaled Interrupts)
- Full-Mini Card (Type F2) form factor

Wide Range of OS Support and Advanced CAN Diagnostic
- Software drivers for Windows® and Linux® included free of charge
- Optional CAN layer 2 software drivers for real-time operating systems
- CANopen®, J1939 and ARINC 825 protocol libraries
- ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology
- High resolution hardware timestamps

Flat Design of CAN Interface Adapter
- Adapter with DSUB9 connector and selectable CAN termination on board

Customization on Request
- Optional extended temperature range -40°C ... +75°C on request

Hardware Designs
The CAN-PCIeMini/402-2 is an add-in PCI Express Full-Mini Card, that features two electrically isolated CAN High-Speed interfaces. The PCI Express® Mini Card CAN-PCIeMini/402-2-FD comes with two CAN FD interfaces. An optional adapter offers a DSUB9 connector and on board CAN termination.

CAN Data Management
The independent CAN nets are driven by the ISO 16845:2004 certified esdACC (esd Advanced CAN Core) implemented in the Altera FPGA. The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU load.

Due to the usage of MSI (Message Signaled Interrupts) the CAN-PCIeMini/402-2(-FD) can be operated for example in Hypervisor environments. The CAN-PCIeMini/402-2(-FD) provides high resolution 64-bit hardware timestamps for CAN messages.

Software Support
Windows and Linux (NTCan-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Realtime OS (NTCan-API)
CAN layer 2 drivers for QNX, RTX(64), VxWorks® and On Time RTOS-32 can be ordered separately.

Higher Layer Protocols
(Classical CAN application only)
Higher Layer Protocols are available for many operating systems (see order info):
- CANopen Master- and Slave-Stack
- J1939
- ARINC825

Additional free-of-charge esd CAN tools for Windows are downloadable from our website. The tools offer efficient setup and analysis of CAN applications and networks.

Customization on Request
Customized options are available for customized serial production in reasonable quantities. Please contact our sales team for detailed information.

Order Information:
Hardware Information:
CAN-PCIeMini/402-2  Active CAN Interface Card for Mini PCI Express, 2x CAN, electrically isolated
Order No. C.2044.04
CAN-PCIeMini/402-2-FD  Active CAN Interface Card for Mini PCI Express, 2x CAN FD, electrically isolated
Order No. C.2044.64

Accessories
- CAN-PCIeMini/402-DSUB9 Adapter with 1x DSUB9 connector, incl. cable, length: 150 mm
Order No. C.2044.10

Software Support
- CAN layer 2 drivers for Windows/Linux are included in delivery free of charge.
- Additional CAN layer 2 object licences including CD-ROM:
  - CANopen Master- and Slave-Stack
  - J1939
  - ARINC825

For detailed information about driver availability for your operating system please contact our sales team.

Technical Specifications:
PCle port PCI Express Spec. R1.0a, Link width 1x
Form factor PCI Express® Mini Card Electromechanical Specification, Revision 1.2
CAN Interface 2 interfaces according to ISO 11898-2, electrical isolation, CAN-PCIeMini/402-2: Bit rates from 10 Kbit/s up to 1 Mbit/s, CAN-PCIeMini/402-2-FD: Bit rates up to 5 Mbit/s

General:
Ambient temp. 0°C ... +75°C
Rel. humidity Max. 90 % (non-condensing)
Power supply 3.3 V: 2x CAN, $I_{\text{max}} = 300 \text{ mA}$, $I_{\text{max}} = 220 \text{ mA}$
Dimensions 30 mm x 51 mm
Connector PCIe: 1x PCIe card edge connector, CAN: 1x 5-pin DSUB per CAN channel, male

Vahrenwalder Str. 207
30165 Hannover / Germany
Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu
CAN-PCIeMini/402-2(-FD)
Driven by esdACC(-FD) (Advanced CAN Core)

Basic Product Features:

- Tested and certified acc. to ISO CAN Conformance Tests “ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan”
- 11-bit and 29-bit CAN IDs
- Supported bit rates:
  - CAN-PCIeMini/402-2: from 10 kbit/s up to 1 Mbit/s
  - CAN-PCIeMini/402-2-FD: up to 5 Mbit/s
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of ‘own’ messages)
- Busload measurement

Superior esdACC Features 1:

- Operating system independently programmable via esd’s NTCAN-API
- 32-bit register interface optimized for CAN needs
- Easy to program
- Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
- On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64 bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - CAN-PCIeMini/402-2: ISO11898-1 conform,
  - Aborted frames in FIFO won’t be blocked by low priority TX

Superior esdACC Features (continued) 1:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer’s needs, including optional integration with customer’s FPGA content
- The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.

1 Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.