XMC-CPU/2041

XMC/PMC Quad Core PowerPC™ CPU with FPGA

XMC-CPU/2041 is shipped with mounted heat sink.

Hardware Manual

to Product V.2029.01

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N O T E

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Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Revision	Chapter	Changes versus previous version	Date
1.0	-	First English manual	2014-03-13
1.1	7.1	Note to bootloader source changed	2014-03-14
1.2	-	Notes “Conformity” and “Data Safety” inserted in Safety Instructions	2014-12-01
1.3	1.	Block circuit diagram new, description of options deleted	2015-04-15
	3.	Description of o-ring mounting inserted	
	4.1	Maximum absolute power inserted	
	4.2	Values of EEPROM and DDR3 RAM changed	
	4.3	Description of optional interfaces deleted,	
	4.12	Chapter Software Support, Chapter Serial Interfaces via P14 (Option) deleted	
	8.	Order Information revised	
1.4	2.2	Figure 2 new	2015-06-23
	2.3	Figure 3 new	
	5.6	New chapter, description of X900 adapters	
	5.7	New chapter, description of X400 adapter	
	8.	Order Information, adapters inserted	

Technical details are subject to change without further notice.

Safety Instructions

- When working with the XMC-CPU/2041 follow the instructions below and read the manual carefully to protect yourself from injury and the XMC-CPU/2041 from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- The device has to be securely installed in the control cabinet before commissioning.
- Protect the XMC-CPU/2041 from dust, moisture and steam.
- Protect the XMC-CPU/2041 from shocks and vibrations.
- The XMC-CPU/2041 may become warm during normal use. Always allow adequate ventilation around the XMC-CPU/2041 and use care when handling.
- Do not operate the XMC-CPU/2041 adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.
- Do not use damaged or defective cables to connect the XMC-CPU/2041.
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The XMC-CPU/2041 may only be driven by power supply current circuits, that are contact protected.
  A power supply, that provides a safety extra-low voltage (SELV or PELV) according to EN 60950-1, complies with this conditions.

Attention !
Electrostatic discharges may cause damage to electronic components.
To avoid this, please perform the steps described on page 10 *before* you touch the XMC-CPU/2041, in order to discharge the static electricity from your body.

Qualified Personal
This documentation is directed exclusively towards personal qualified in control and automation engineering.
The installation and commissioning of the product may only be carried out by qualified personal, which is authorized to put devices, systems and electric circuits into operation according to the applicable national standards of safety engineering.

Conformity
This device is a sub-assembly intended for incorporation into an apparatus by a manufacturer and NOT by the end user. The manufacturer of the final system must decide, whether additional EMC or EMI protection requirements are necessary.

Data Safety
This device is equipped with an Ethernet or other interface which is suitable to establish a connection to data networks. Depending on the software used on the device, these interfaces may allow attackers to compromise normal function, get illegal access or cause damage.
esd does not take responsibility for any damage caused by the device if operated at any networks. It is the responsibility of the device's user to take care that necessary safety precautions for the device's network interface are in place.

Intended Use
The intended use of the XMC-CPU/2041 is the operation as XMC/PMC Quad Core PowerPC™ CPU with FPGA.
The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The XMC-CPU/2041 is intended for installation on a base board according to IEEE 1386.1-2001 (PMC) or Vita 42.3 (XMC).
- The operation of the XMC-CPU/2041 in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the XMC-CPU/2041 for medical purposes is prohibited.

Service Note
The XMC-CPU/2041 does not contain any parts that require maintenance by the user. The XMC-CPU/2041 does not require any manual configuration of the hardware.

Disposal
Devices which have become defective in the long run have to be disposed in an appropriate way or have to be returned to the manufacturer for proper disposal. Please, make a contribution to environmental protection.

Table of contents

1. Overview

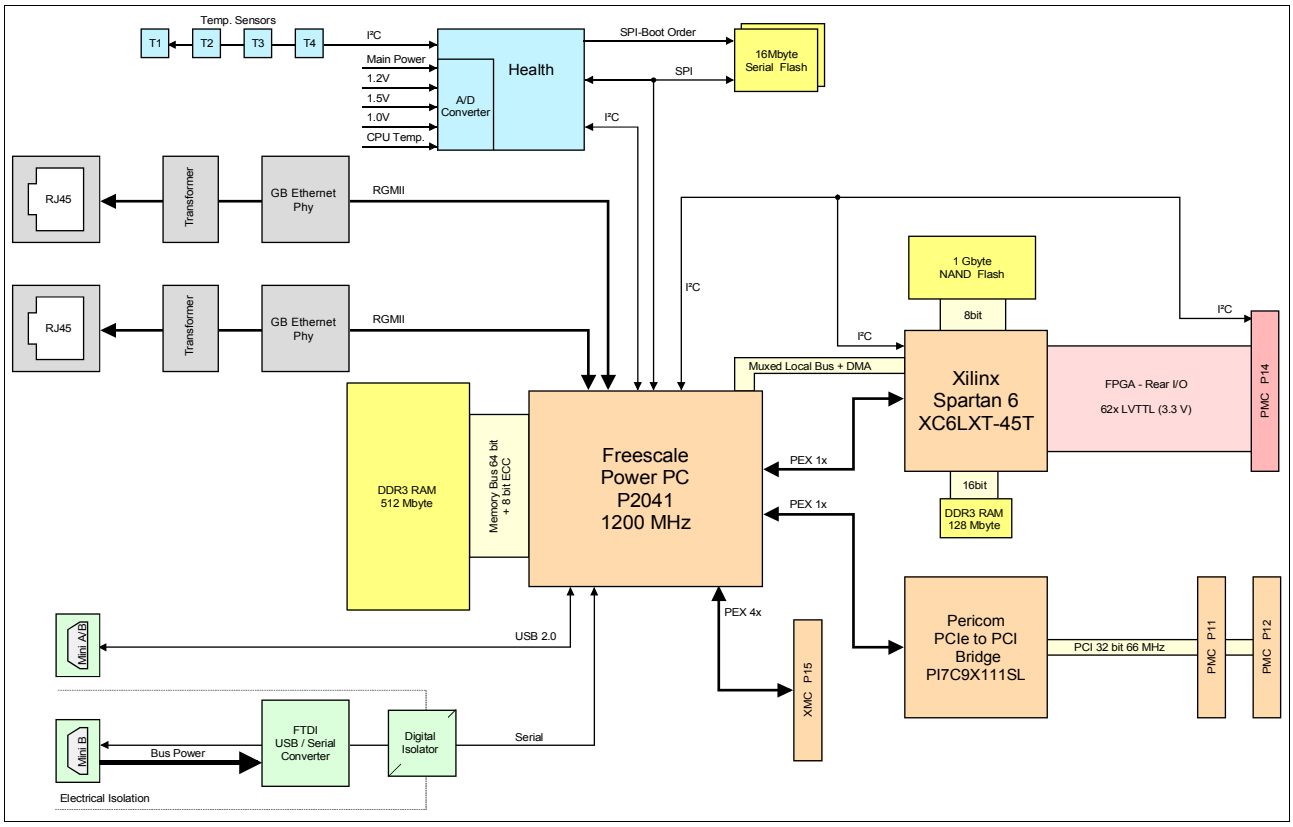


Figure 1: Block circuit diagram

The XMC-CPU/2041 is an XMC PowerPC Host CPU.
It is a equipped with a PMC and an XMC interface.
The powerful Freescale™ PowerPC™ QorIQ P2041 with 1.2 GHz is built on Power Architecture® technology, bringing high-end architectural features pioneered in the P4 platform into the mid range quad core space.
The local memory bus is 64 bits wide plus 8 bits ECC with an overall capacity of 512 Mbyte. 16 Mbyte SPI Flash for boot loader and 32 Kbit I²C EEPROM for U-Boot environment offer non-volatile memory spaces.
The XMC-CPU/2041 is equipped with a second 16 Mbyte “fallback” SPI Flash that is used for system recovery, if a system crash occurs during a firmware update.

The Xilinx® FPGA Spartan® 6 is connected to the CPU by local bus for low latency data exchange. For high bandwidth data exchange the FPGA is additionally connected via PCI Express to the CPU. 62 LVTTL-I/Os of the FPGA are routed to the PMC-P14 connector.

The XMC interface comes with 4-lane PCIe bus and is designed according to VITA 42.3.
The PMC interface supports 32 bit / 66 MHz PCI bus according to PCI Local Bus Specification 3.0, 3.3 V voltage level (5 V tolerant) and PCI bus master capability.

The XMC-CPU/2041 is equipped with two Gigabit Ethernet interfaces accessible at the front panel, which give an excellent base for EtherCAT® applications.
The USB host port supports USB 2.0.

2. XMC-CPU/2041 View with Connectors and LEDs

2.1 PCB Top Layer View with Connectors and LEDs

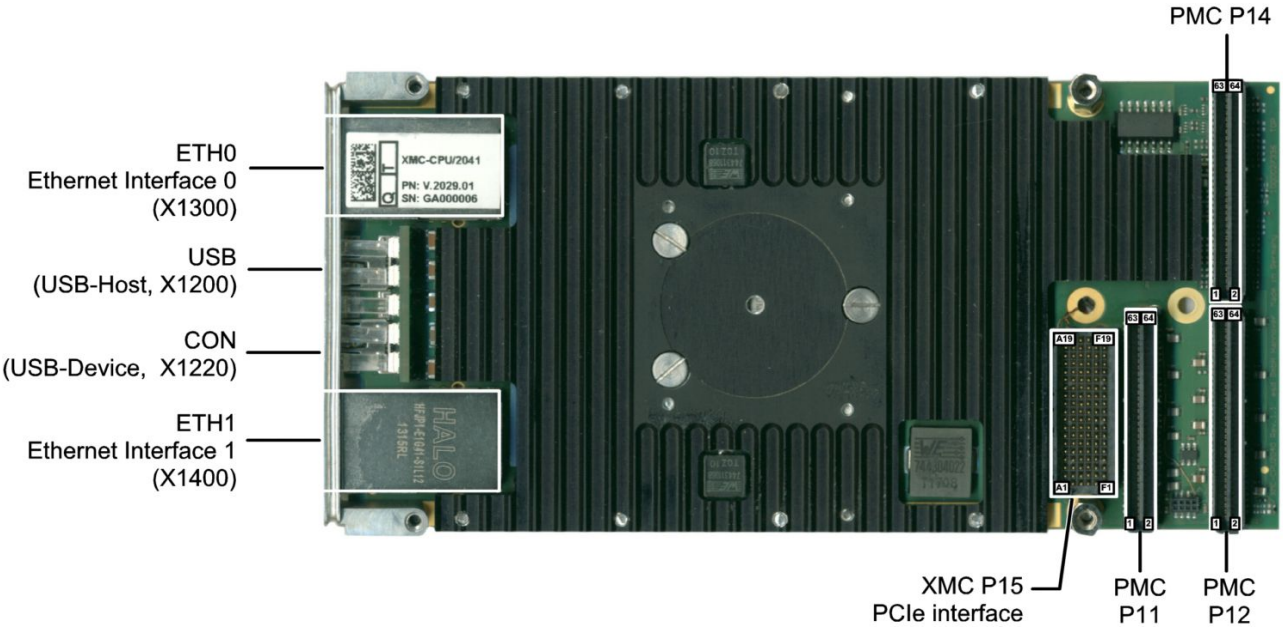


Figure 2: PCB top view

See also page 16 and following for signal assignments of the connectors.
The JTAG connector and the Debug interface connector have to be connected on the PCB bottom side of XMC-CPU/2041 (see Figure 3 for the position of the connectors and pins).

2.2 PCB Bottom Layer View with LEDs, JTAG and Debug Interface

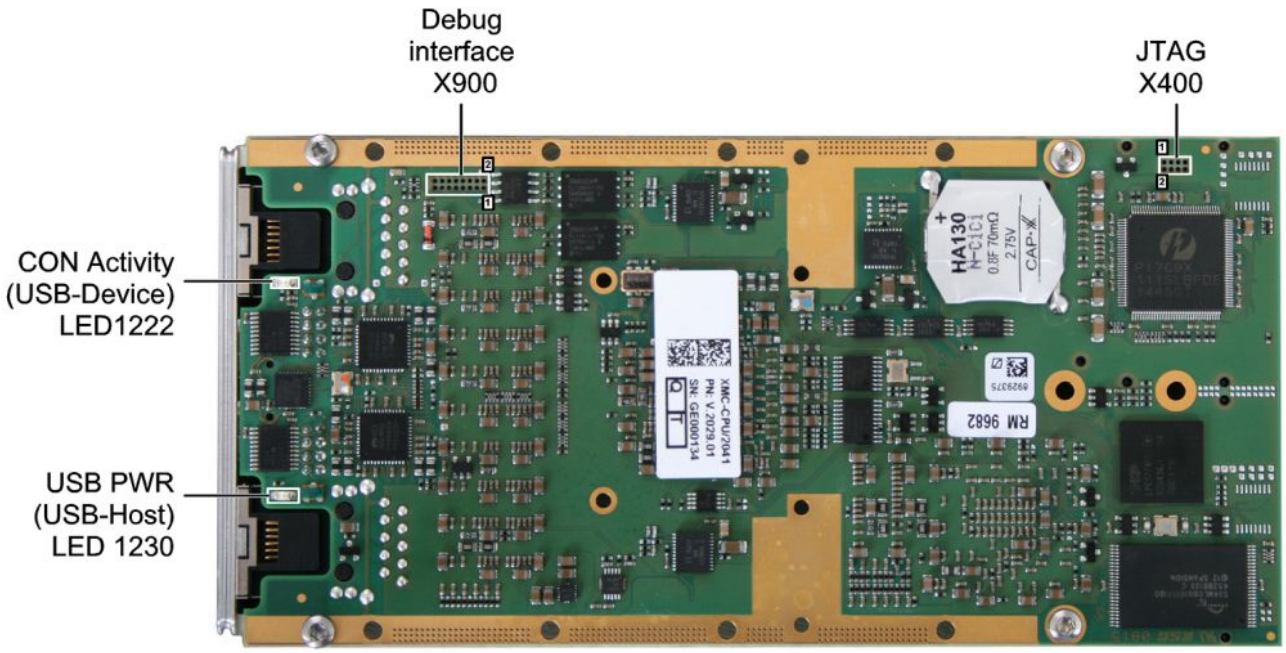


Figure 3: PCB bottom view

The Debug interface and the JTAG interfaces have to be connected from the bottom side of the XMC-CPU/2041. See also page 16 and following for signal assignments of the connectors.
esd offers special adapters as accessories, see “Order Information” on page 29.

2.2.1 Indication of CON Activity (LED 1222) and USB PWR (LED1230)

LED	Colour	Indication	Description (LED on)	LED name in schematic diagram
CON Activity	green	Activity	Data transfer on terminal interface CON	LED1222
USB PWR	green	Power	5 V power supply voltage of USB interface on	LED1230

Table 1: LEDs CON Activity and USB PWR

2.3 Front Panel View with Connectors and LEDs

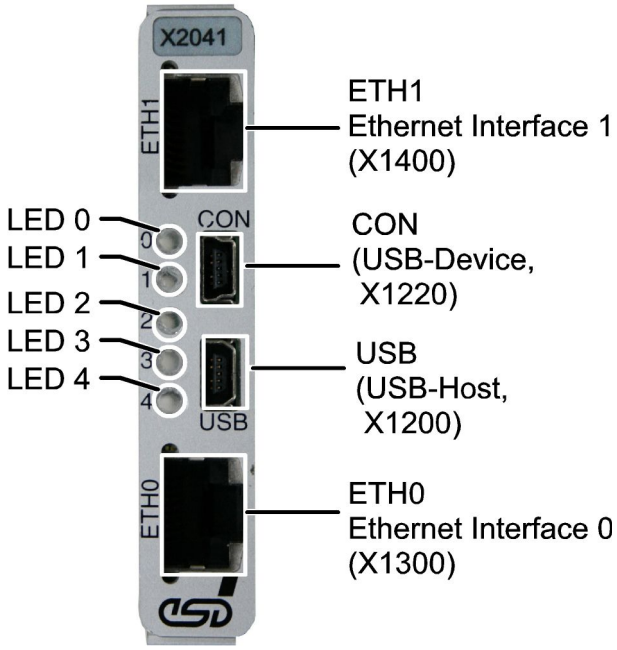


Figure 4: Front panel view

2.3.1 LED0-4 Indication of the TriColor LEDs

Five TriColor LEDs are equipped in the front panel.

LED	Colour	Description	Signal name in schematic diagram
LEDX	green	User-defined via FPGA and driver	LED10XG
	red		LED10XR
	blue		LED10XB

(X = 0-4)

Table 2: LEDs 0 - 4

3. Hardware Installation

Read the safety instructions at the beginning of this document carefully, before you start with the hardware installation!

Danger!
Electric shock risk. Never carry out work while power supply voltage is switched on!

Attention !
Electrostatic discharges may cause damage to electronic components.
To avoid this, please discharge the static electricity from your body *before* you touch the XMC-CPU/2041.

Procedure:

1. Switch off your system and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. Disconnect the system from the mains.
   If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (i.e. with caution label).

   Danger!
   Never carry out work while power supply voltage is switched on!
4. Open the case if necessary.
5. For sufficient EMC shielding the XMC-CPU/2041 should make contact to the system's enclosure nearly completely around its front panel. For this purpose a conductive O-ring is contained in the product package of the XMC-CPU/2041 module. Mount the conductive O-ring on the front panel of the XMC-CPU/2041. Additionally or instead of it use shielding material as for example conductive shielding gasket.
6. Remove the carrier board (if already installed) and plug the XMC-CPU/2041 carefully on the carrier board. Pay attention that the XMC-CPU/2041 is correctly installed on the carrier board.
   Fix the XMC-CPU/2041 with the screws on the carrier board. Use the four M 2.5 x 6 mm screws which are contained in the product package of the module.
7. Install the carrier board in your system.
8. Close the case again (if necessary).
9. Connect the Ethernet and the USB interfaces via the connectors in the front panel of the XMC-CPU/2041.
10. Connect the system to mains again (mains connector or safety fuse).
11. Switch on the system and the peripheral devices.
12. End of hardware installation.
    Set the interface properties in your operating system. Refer to the documentation of the operating system.

4. Technical Data

4.1 General Technical Data

Power supply voltage	Nominal voltage:	depending on slot used: **PMC interface:** 3.3 V / $I_{3.3V\_MAX}$ = 2.5 A, $I_{3.3V\_TYPICAL}$ = 2.2 A, 5V / I_{5V_MAX} = 3 A, $I_{5V\_TYPICAL}$ = 2.5 A **XMC interface:** 3.3 V / $I_{3.3V\_MAX}$ = 2.5 A, $I_{3.3V\_TYPICAL}$ = 2.2 A, 12V / I_{12V_MAX} = 1.5 A, $I_{12V\_TYPICAL}$ = 1.2 A Absolute maximum power: $P_{3.3V+5V\_MAX}$ = 19 W
Connectors	ETH0 ETH1	RJ45 socket (X1300) - Ethernet Port 0 RJ45 socket (X1400) - Ethernet Port 1
	CON	Mini USB socket type-B (X1220) - Console (USB-Device)
	USB	Mini USB socket type-AB (X1200) - USB-Host
	PMC P11 PMC P12 PMC P14 XMC P15	64-pin PMC connector (P11) - PMC PCI part 1 64-pin PMC connector (P12) - PMC PCI part 2 64-pin PMC connector (P14) - PMC IO XMC, Samtec ASP-105885-04 - PCI Express interface
	Only for test- and programming purposes:	
	Debug	internal connector (under the heat sink), has to be connected from the bottom side of the XMC-CPU/2041. Samtec CLM108-02-F-D-BE (pass-thru micro socket, X900) - Debug interface of the CPU and the Health Controller
	JTAG	Samtec CLM104-02-F-D-BE (pass-thru micro socket, X400), has to be connected from the bottom side of the XMC-CPU/2041. - JTAG interface additionally via XMC-P11 and P12
Temperature range	Operating temperature: -40 °C ... + 65 °C (600 LFM) Storage temperature: -40 °C ... +105 °C ambient	
Humidity	0% ... 90%, non-condensing	
Dimensions	149 mm x 74 mm	
Weight	190 g	

Table 3: General data of the module

4.2 CPU and Memory

CPU	Freescale PowerPC QorIQ P2041, 1.2 GHz, e500mc core double precision floating point unit
RAM	512 Mbyte RAM 64-bit wide plus 8 bits ECC DDR3 RAM
Flash memory (SPI)	16 Mbyte SPI FLASH for boot loader (standard) and 16 Mbyte SPI FLASH for system recovery, selected via Health Subsystem.
EEPROM	1x 32 Kbit I²C EEPROM for U-Boot environment, 1x 4 Kbit RAM SPD, 1x 32 Kbit EEPROM for Bootstrapping
NAND Flash	1 Gbyte NAND Flash for operating system connected via FPGA
DDR3 RAM on FPGA	128 Mbyte RAM connected to FPGA for FPGA usage, with 16-bit wide interface

Table 4: CPU and memory

4.3 Ethernet Interface

Number of Ethernet interfaces	2x Gigabit Ethernet (ETH0, ETH1)
Standard	IEEE 802.3, 10BASE-T, 100BASE-TX, 1000BASE-T
Bit rate	10/100/1000 Mbit/s
Connection	Twisted Pair (compatible to IEEE 802.3),
Electrical isolation	Via transformer, 1500Vrms / 2250 VDC
Connector	2x at RJ-45-socket in the front panel

Table 5: Data of the Ethernet interfaces

4.4 USB, USB Host Interface

Number	1x USB host
Standard	USB 2.0, max. 480 Mbit/s
Topology	Host Controller integrated in CPU
Max. current per port @5V	500 mA, short-circuit-protected
Electrical isolation	None
Software support	- OHCI-Host controller- and device driver - driver of the operating system
Connector	Mini USB type-AB socket in the front panel (USB)

Table 6: Data of the USB Host interface USB

4.5 CON, USB Device Interface

Number	1x Console (serial)
Standard	USB 2.0 Full-Speed, the first serial interface of the CPU is provided via an FTDI FT232R chip as USB Device. The FT232R chip is supplied by USB.
Electrical isolation	Via digital isolator
Connector	Mini USB type-B socket in the front panel (CON)

Table 7: Data of the USB Device interface CON

4.6 PMC Interface

Standard	PCI bus according to PCI Local Bus Specification 3.0, 32 bit 33/66 MHz, PCI bus master capability
Voltage	3.3 V, (5 V tolerant)
Frequency	33/66 MHz
Mode	Monarch / non Monarch
Connector	Via PMC P11 and PMC P12
Device ID / Vendor ID	Constant 0x0410 / 0x1957
Subsystem Device ID / Subsystem Vendor ID	0x0700 / 0x12FE as endpoint

Table 8: Data of the PMC interface

4.7 XMC Interface

Standard	XMC according to VITA 42.3, 4-lane PCI EXPRESS® acc. to PCIe 1.1
Lanes	4
Mode	As device
Connector	Via XMC P15
Device ID / Vendor ID	Constant, 0x0410 / 0x1957
Subsystem Device ID / Subsystem Vendor ID	0x0701 / 0x12FE as endpoint

Table 9: Data of the XMC interface

4.8 I²C Interface

Number	3x I²C interface - 1x for external use, - 2x for internal use only!
Control	Integrated in CPU
Bit rate	100Kbit, optional 400 Kbit
Physical Interface	3.3 V only, not 5 V tolerant.
1. I2C interface	Devices: CPU Setup EEPROM, DDR3 RAM SPD EEPROM, RTC
2. IC2 interface	Devices: PCIe to PCI Bridge, Health controller, U-Boot Env EEPROM.
3. I2C interface	Devices: FPGA, connector P14 pin 63 SDA pin 64 SCL.

Table 10: Data of the I²C interface

4.9 Real-Time Clock (RTC)

Type	Epson RX8025SA
Connection	I^2C Bus
Accuracy	+/-5 ppm at T_{amb} = 25 °C (< 30 s/month)
Buffer	Goldcap, C = 0,8 F

Table 11: Microprocessor and Memory

4.10 Digital In-/Outputs

Number	62x LVTTL-IO
I/O-configuration	As input or output configurable pins of the FPGA
Input switching threshold	LVTTL 3.3 V // not 5V tolerant
Output current	Depending on FPGA configuration, see XILINX data sheet
Electrical isolation	None
Protection circuit	None, current-limiting resistors are not provided.
Connector	XMC-P14

Table 12: Data of the digital in-/outputs

4.11 Health

System for monitoring of the board's status.

Voltages	Core voltage:	0.75 V, 1.0 V, 1.2 V,	1.5 V, 2.5 V, 3.3 V,	5 $V_{\_USB}$, 5 $V_{\_PMC}$, XMC_VPWR
Temperature monitor	4x I²C temperature sensors, 1x CPU integrated temperature diode			
XMC-IPMI Support	Data according to „IPMI Serial EEPROM FRU Information“			
Boot	Selection of the SPI FLASH for booting, GPIO expander for various control functions			

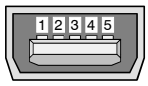
4.12 Software Support

The flash memory carries the standard boot program U-boot and enables the XMC-CPU/2041 to boot various operating systems from network or on-board SPI-Flash.
BSPs are available for VxWorks® and Linux®. Example source code for the FPGA is included in the BSPs.
For the FPGA an esdACC (esd Advanced CAN Controller) implementation is available.

5. Connector Assignments

5.1 USB, (USB Host, X1200)

Device connector: 5-pin mini USB socket, standard type AB

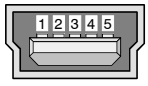
Pin Position:	Pin Assignment:	
	**Pin**	**CON (X1220)**
	1	V_{BUS}
	2	D-
	3	D+
	4	UID
	5	GND

Signal Description:

V_{BUS}... +5 V power supply voltage
D+, D-... USB signal lines Data+, Data-
UID... Signal to distinguish between a host connection and a device connection:
- host connection: signal connected to the signal ground
- device connection: not connected
GND... Reference potential

5.2 CON, (USB Device, X1220)

Device connector: 5-pin mini USB socket, standard type B

Pin Position:	Pin Assignment:	
	**Pin**	**CON (X1220)**
	1	V_{BUS}
	2	D-
	3	D+
	4	-
	5	GND

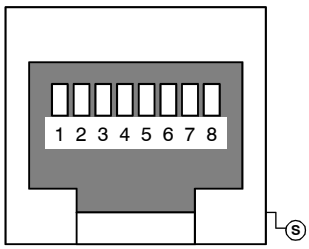
Signal Description:

V_{BUS}... +5 V power supply voltage
D+, D-... USB signal lines Data+, Data-
-... not connected
GND... Reference potential

5.3 Ethernet ETH0, ETH1

Device connector: RJ45 socket, 8-pin

Pin Position:



Pin Assignment:

Pin	Signal
1	MDI0+ (TP0+)
2	MDI0- (TP0-)
3	MDI1+ (TP1+)
4	MDI2+ (TP2+)
5	MDI2- (TP2-)
6	MDI1- (TP1-)
7	MDI3+ (TP3+)
8	MDI3- (TP3-)

S	Shield

Signal Description:

MDIx+, MDIx- ... Ethernet data lines (x = 0 - 3)
Shield... case shield, connected with the front panel of the XMC-CPU/2041.

Note:
Cables of category CAT5e or higher have to be used to grant the function in networks with 1000 Mbit/s.

5.4 PMC Connectors

The XMC-CPU/2041 uses the PMC connectors P11, P12 and P14.
The assignment of the connectors P11 and P12 is in accordance with IEEE1386.
P14 is assigned module-specific.

5.4.1 PMC P11 Connector

Pin	Signal	Signal	Pin
1	TCK	-12V	2
3	GND	INTA#	4
5	INTB#	INTC#	6
7	GND (PRESENT#)	+5V	8
9	INTD#	n.c. (reserved)	10
11	GND	PMCAUX	12
13	PCI-CLK_IN	GND	14
15	GND	GNT#	16
17	REQ#	+5V	18
19	VIO	AD[31]	20
21	AD[28]	AD[27]	22
23	AD[25]	GND	24
25	GND	C/BE3#	26
27	AD[22]	AD[21]	28
29	AD[19]	+5V	30
31	VIO	AD[17]	32
33	FRAME#	GND	34
35	GND	IRDY#	36
37	DEVSEL#	+5V	38
39	GND (PCIXCAP#)	PCI_LOCK#	40
41	n.c. (SDONE#)	n.c. (SBO#)	42
43	PAR	GND	44
45	VIO	AD[15]	46
47	AD[12]	AD[11]	48
49	AD[09]	+5V	50
51	GND	C/BE0#	52
53	AD[06]	AD[05]	54
55	AD[04]	GND	56
57	VIO	AD[03]	58
59	AD[02]	AD[01]	60
61	AD[00]	+5V	62
63	GND	n.c. (REQ64#)	64

5.4.2 PMC P12 Connector

Pin	Signal	Signal	Pin
1	+12V	TRST#	2
3	TMS	TDO	4
5	TDI	GND	6
7	GND	n.c. (reserved)	8
9	n.c. (reserved)	n.c. (reserved)	10
11	n.c. (MODE2#)	+3.3V	12
13	PCI-RST#	n.c. (MODE3#)	14
15	+3.3V	n.c. (MODE4#)	16
17	PME#	GND	18
19	AD[30]	AD[29]	20
21	GND	AD[26]	22
23	AD[24]	+3.3V	24
25	IDSEL	AD[23]	26
27	+3.3V	AD[20]	28
29	AD[18]	GND	30
31	AD[16]	C/BE2#	32
33	GND	n.c. (IDSELB)	34
35	TRDY#	+3.3V	36
37	GND	STOP#	38
39	PERR#	GND	40
41	+3.3V	SERR#	42
43	C/BE1#	GND	44
45	AD[14]	AD[13]	46
47	M66EN	AD[10]	48
49	AD[08]	+3.3V	50
51	AD[07]	n.c. (REQB#)	52
53	+3.3V	n.c. (GNTB#)	54
55	n.c. (reserved)	GND	56
57	n.c. (reserved)	EREADY	58
59	GND	RESETOUT#	60
61	n.c. (ACK64#)	+3.3V	62
63	GND	MONARCH#	64

5.4.3 PMC P14 I/O Connector

Standard Pin Assignment			Optional Pin Assignment			
Pin	**Signal Name**	**Notes**	**Alternative Signal Name***	**Notes***	**Differential Pair* (XILINX Name)**	**Notes***
1	FPGA-IO<0>	3.3V, IO	SGMII-RX-N-<0>	LVDIFF	74-N	3xSGMII option only
2	FPGA-IO<1>	3.3V, IO	SGMII-TX-P-<1>	LVDIFF	61-N	3xSGMII option only
3	FPGA-IO<2>	3.3V, IO	SGMII-RX-P-<0>	LVDIFF	74-P	3xSGMII option only
4	FPGA-IO<3>	3.3V, IO	SGMII-TX-N-<1>	LVDIFF	61-P	3xSGMII option only
5	FPGA-IO<4>	3.3V, IO	GND (when using SGMII 0 or 1)	GND	60-N	3xSGMII option only
6	FPGA-IO<5>	3.3V, IO	SGMII-RX-P-<1>	LVDIFF	53-N	3xSGMII option only
7	FPGA-IO<6>	3.3V, IO	GND (when using SGMII 0 or 1)	GND	60-P	3xSGMII option only
8	FPGA-IO<7>	3.3V, IO	SGMII-RX-N-<1>	LVDIFF	53-P	3xSGMII option only
9	FPGA-IO<8>	3.3V, IO	SGMII-TX-N-<0>	LVDIFF	52-N	3xSGMII option only
10	FPGA-IO<9>	3.3V, IO	SGMII-RX-N-<2>	LVDIFF	51-N	1 and 3xSGMII option only
11	FPGA-IO<10>	3.3V, IO	SGMII-TX-P-<0>	LVDIFF	52-P	3xSGMII option only
12	FPGA-IO<11>	3.3V, IO	SGMII-RX-P-<2>	LVDIFF	51-P	1 and 3xSGMII option only
13	FPGA-IO<12>	3.3V, IO	SGMII-TX-P-<2>	LVDIFF	50-N	1 and 3xSGMII option only
14	FPGA-IO<13>	3.3V, IO	GND (when using SGMII 0,1 or 2)	GND	49-N	1 and 3xSGMII option only
15	FPGA-IO<14>	3.3V, IO	SGMII-TX-N-<2>	LVDIFF	50-P	1 and 3xSGMII option only
16	FPGA-IO<15>	3.3V, IO	GND (when using SGMII 0,1 or 2)	GND	49-P	1 and 3xSGMII option only
17	FPGA-IO<16>	3.3V, IO	GND (when using SGMII 0,1 or 2)	GND	48-N	1 and 3xSGMII option only
18	FPGA-IO<17>	3.3V, IO	GND (when using SGMII 0,1 or 2)	GND	47-N	1 and 3xSGMII option only
19	FPGA-IO<18>	3.3V, IO			48-P	
20	FPGA-IO<19>	3.3V, IO	ETH-MDC	3.3V, IO	47-P	when using one of both SGMII options
21	FPGA-IO<20>	3.3V, IO			46-N	
22	FPGA-IO<21>	3.3V, IO	ETH-MDIO	3.3V, IO	45-N	when using one of both SGMII options
23	FPGA-IO<22>	3.3V, IO			46-P	
24	FPGA-IO<23>	3.3V, IO	ETHINT3#	3.3V, IO	45-P	when using one of both SGMII options
25	FPGA-IO<24>	3.3V, IO			44-N	
26	FPGA-IO<25>	3.3V, IO			43-N	CLK Input
27	FPGA-IO<26>	3.3V, IO			44-P	
28	FPGA-IO<27>	3.3V, IO			43-P	CLK Input
29	FPGA-IO<28>	3.3V, IO			42-N	CLK Input
30	FPGA-IO<29>	3.3V, IO			41-N	CLK Input
31	FPGA-IO<30>	3.3V, IO			42-P	CLK Input
32	FPGA-IO<31>	3.3V, IO			41-P	CLK Input

* The optional pin assignment is only available on request.

Standard Pin Assignment			Optional Pin Assignment			
Pin	**Signal Name**	**Notes**	**Alternative Signal Name***	**Notes***	**Differential Pair* (XILINX Name)**	**Notes***
33	FPGA-IO<32>	3.3V, IO			40-N	CLK Input
34	FPGA-IO<33>	3.3V, IO	CAN0_Tx	3.3V, O	39-N	
35	FPGA-IO<34>	3.3V, IO			40-P	CLK Input
36	FPGA-IO<35>	3.3V, IO	CAN0_Rx	5V, I	39-P	
37	FPGA-IO<36>	3.3V, IO			38-N	
38	FPGA-IO<37>	3.3V, IO	CAN1_Tx	3.3V, O	37-N	
39	FPGA-IO<38>	3.3V, IO			38-P	
40	FPGA-IO<39>	3.3V, IO	CAN1_Rx	5V, I	37-P	
41	FPGA-IO<40>	3.3V, IO			36-N	
42	FPGA-IO<41>	3.3V, IO	GND (when using CAN 0 or 1)	GND	35-N	
43	FPGA-IO<42>	3.3V, IO	GND (when using CAN 0 or 1)	GND	36-P	
44	FPGA-IO<43>	3.3V, IO	Tx_S0	RS232, O	35-P	
45	FPGA-IO<44>	3.3V, IO			34-N	
46	FPGA-IO<45>	3.3V, IO	Rx_S1 or Rx_S2	RS232, I	33-N	
47	FPGA-IO<46>	3.3V, IO	RTS_S1 or Tx_S3	RS232, O	34-P	
48	FPGA-IO<47>	3.3V, IO	Tx_S1 or Tx_S2	RS232, O	33-P	
49	FPGA-IO<48>	3.3V, IO	CTS_S1 or Rx_S3	RS232, I	32-N	
50	FPGA-IO<49>	3.3V, IO	Rx_S0	RS232, I	31-N	
51	FPGA-IO<50>	3.3V, IO			32-P	
52	FPGA-IO<51>	3.3V, IO	GND (when using SER 1)	GND	31-P	
53	FPGA-IO<52>	3.3V, IO		3.3V, IO	30-N	acc. to Technical Specification: CLOCK_IN
54	FPGA-IO<53>	3.3V, IO	RTS_S0 or Tx_S1	RS232, O	29-N	CLOCK_OUT
55	FPGA-IO<54>	3.3V, IO			30-P	RESET_IN
56	FPGA-IO<55>	3.3V, IO	CTS_S0 or Rx_S1	RS232, I	29-P	RESET_OUT
57	FPGA-IO<56>	3.3V, IO			20-N	IRIG-B_R_IN
58	FPGA-IO<57>	3.3V, IO			19-N	IRIG-B_R_OUT
59	FPGA-IO<58>	3.3V, IO			20-P	IRIG-B_R_P
60	FPGA-IO<59>	3.3V, IO	RS485+	RS485, I	19-P	CLOCK_EN
61	FPGA-IO<60>	3.3V, IO			1-N	IRIG-B_R_M
62	FPGA-IO<62>	3.3V, IO	RS485+	RS485, O	1-P	RESET_EN
63	IIC3-SDA	3.3V, IO				
64	IIC3-SCL	3.3V, O				

* The optional pin assignment is only available on request.

Note:
The signals in the column "Alternative Signal Name" are assembly options that can be switched via 0 Ω resistors on request!

5.5 P15 PCI Express Interface

Pin	Signal					
	Row A	Row B	Row C	Row D	Row E	Row F
19	PEX RCLK IN+	PEX RCLK IN-	n.c.	LC.WAKE#	LC.ROOT#	n.c.
18	GND	GND	n.c.	GND	GND	n.c.
17	n.c.	n.c.	n.c.	n.c.	n.c.	n.c.
16	GND	GND	I²C.WE	GND	GND	I²C.SCL
15	n.c.	n.c.	n.c.	n.c.	n.c.	VPWR
14	GND	GND	I²C.GA2	GND	GND	I²C.4.SDA
13	PEX4 Rx+	PEX4 Rx-	XMC AUX	PEX5 Rx+	PEX5 Rx-	VPWR
12	GND	GND	I²C.GA1	GND	GND	GND
11	PEX2 Rx+	PEX2 Rx-	n.c.	PEX3 Rx+	PEX3 Rx-	VPWR
10	GND	GND	X0.TDO	GND	GND	I²C.GA0
9	n.c.	n.c.	n.c.	n.c.	n.c.	VPWR
8	GND	GND	X0.TDI	GND	GND	- 12V
7	n.c.	n.c.	3.3 V	n.c.	n.c.	VPWR
6	GND	GND	X0.TMS	GND	GND	+12 V
5	n.c.	n.c.	3.3 V	n.c.	n.c.	VPWR
4	GND	GND	X0.TCK	GND	GND	LC.RST0#
3	PEX4 Tx+	PEX4 Tx-	3.3 V	PEX5 Tx+	PEX5 Tx-	VPWR
2	GND	GND	X0.TRST#	GND	GND	LC.PERST#
1	PEX2 Tx+	PEX2 Tx-	3.3 V	PEX3 Tx+	PEX3 Tx-	VPWR

5.6 JTAG X900

The JTAG interface has to be connected from the bottom side of the XMC-CPU/2041. esd offers two adapters, the XMC-CPU/2041-ADAPTER-BDI and the XMC-CPU/2041-ADAPTER-NXP as accessories. See Order Information on page 29 for more detail.

5.6.1 XMC-CPU/2041-ADAPTER-BDI

The XMC-CPU/2041-ADAPTER-BDI (esd order No.: V.2029.02) is an interface to connect the Abatron BDI2000 or BDI3000 debugger to the XMC-CPU/2041 connector X900.

Samtec CLM (16 pins) <-> box header (16 pins)

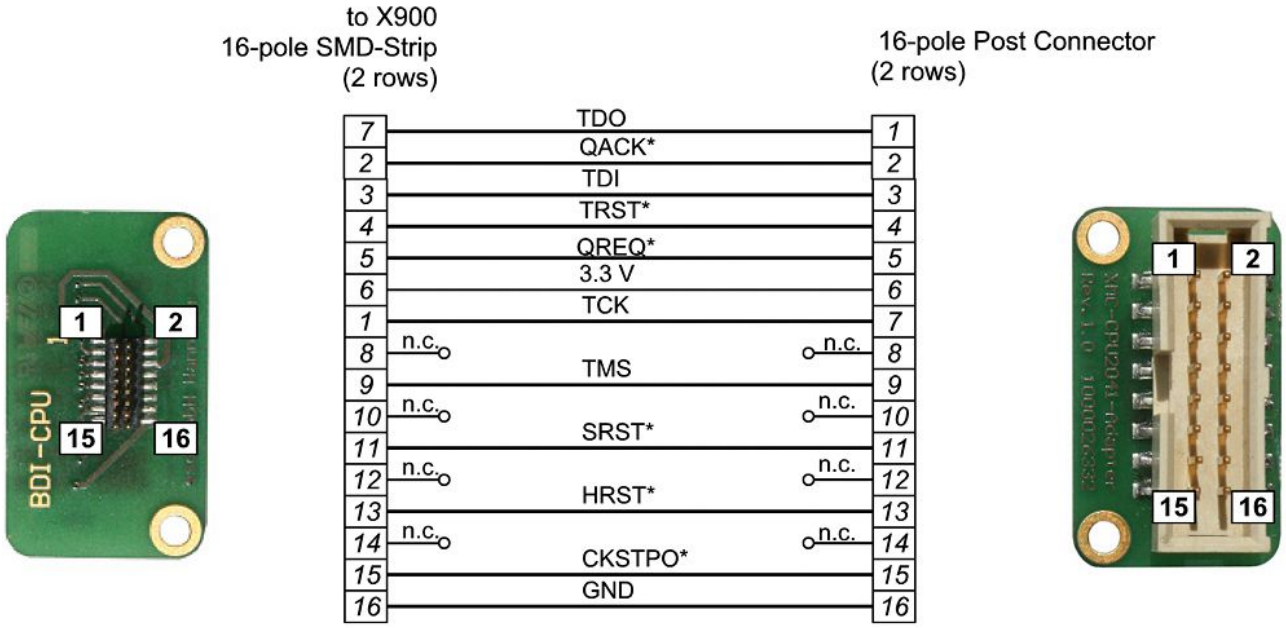


Figure 5: XMC-CPU/2041-ADAPTER-BDI

Notice:
The 16-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 3 on page 8 for the position of the X900 connector pins.

5.6.2 XMC-CPU/2041-ADAPTER-NXP

The XMC-CPU/2041-ADAPTER-NXP (esd order No.: V.2029.04) is an interface to connect the NXP (Health Controller) to the XMC-CPU/2041 connector X900.

Samtec CLM (16 pins) <-> box header (6 pins)

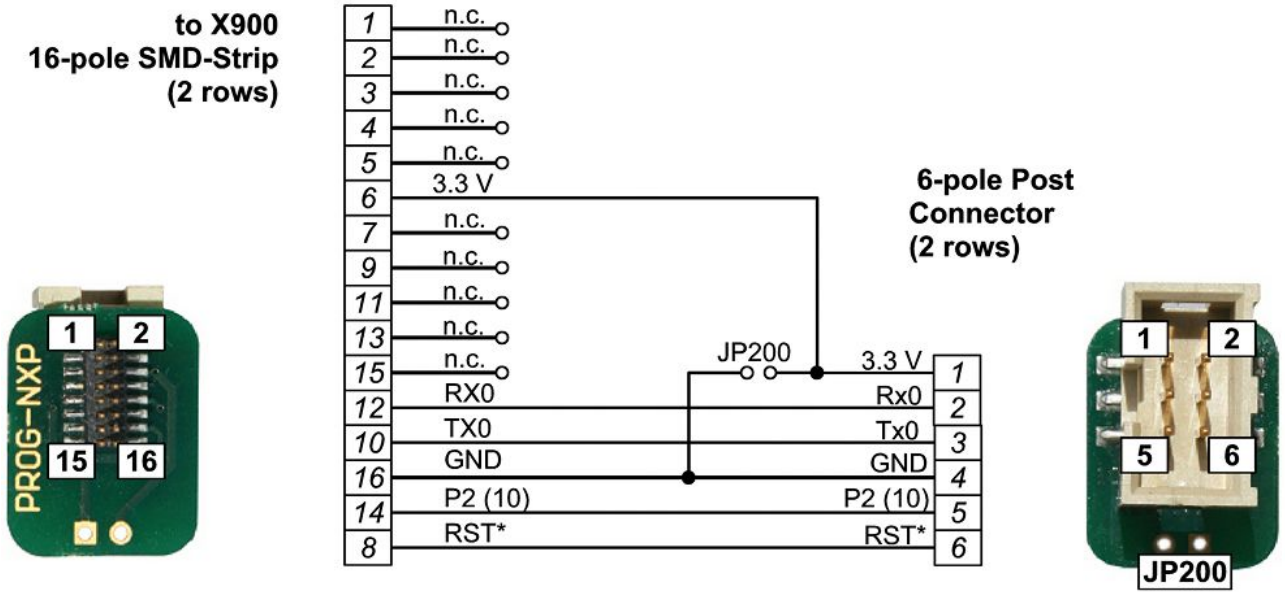


Figure 6: XMC-CPU/2041-ADAPTER-NXP

Notice:
The 16-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 3 on page 8 for the position of the X900 connector pins.

5.7 Debug Interface X400

The Debug interface has to be connected from the bottom side of the XMC-CPU/2041. esd offers the XMC-CPU/2041-ADAPTER-FPGA as accessory, see Order Information on page 29.

5.7.1 XMC-CPU/2041-ADAPTER-FPGA

The XMC-CPU/2041-ADAPTER-FPGA (esd order No.: V.2029.03) is an interface to connect the Tool XILINX ChipScope to the XMC-CPU/2041 connector X400.

Samtec CLM (8 pins)	<->	box header (10 pins)

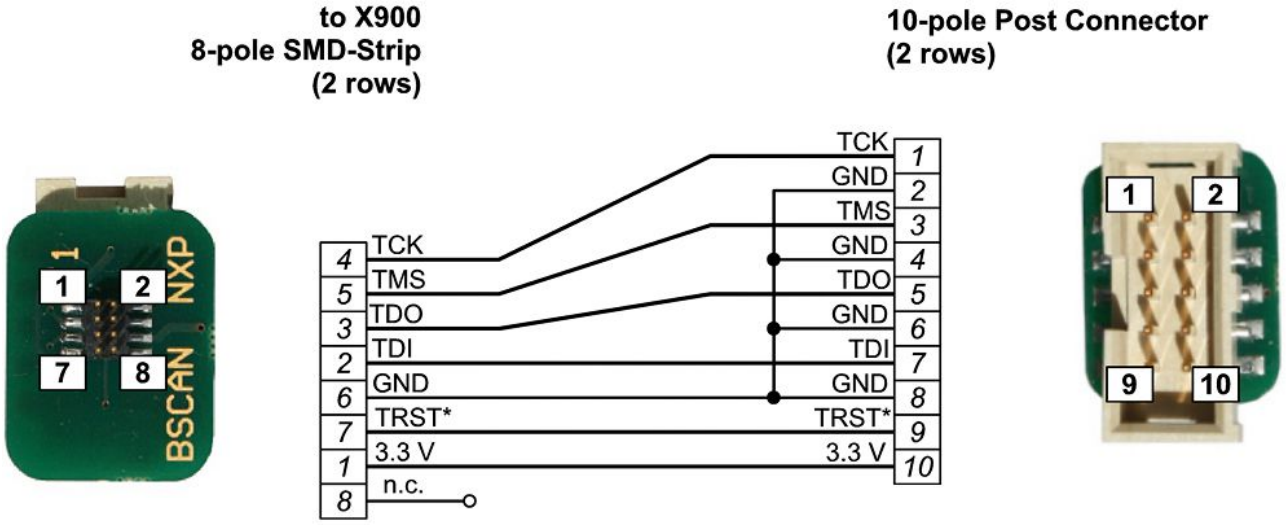


Figure 7: XMC-CPU/2041-ADAPTER-FPGA

Notice:
The 8-pole SMD strip has no inverse-polarity protection! Property damage may result due to incorrect adapter connection.
Ensure that the connector is plugged in in the right position. See figure 3 on page 8 for the position of the X400 connector pins.

6. FPGA

Interface to CPU	16 bit at the enhanced Local Bus of the P2041 (75 MHz)
	PCI Express with one Lane
	I²C
	1 DMA channel (DMA Req, DMA Ack, DMA Done).
	2 Interrupts.
	Control of the TriColor LED's in the front panel
Interface to connector P4	See chapter 5.4.3
Example/Test Code	16-bit enhanced Local Bus interface incl. 32-bit access
	PCI Express interface, as device and master
	NAND FLASH interface.
	Control of the TriColor LED's in the front panel
	FIFO 32 bits wide

7. Bootloader

7.1 License

The XMC-CPU/2041 module uses the opensource bootloader *„Das U-Boot“*. The U-Boot source-code is published in terms of the GNU public license (GPL). Please see esd's „3rd party licensor notice“ document that is part of the product's documentation for the full license text. You can contact esd for a copy of the full bootloader sourcecode for the XMC-CPU/2041.
The U-Boot source is available from esd on request.

7.2 Configuration and Console Access

Use an USB cable with mini-B connector (XMC-CPU/2041 side) and type A connector (PC side) to connect the XMC-CPU/2041 to a PCs USB port. The U-Boot console is accessible via the front panel's USB 'CON' device port (mini-B socket). After the first connection of the PMC module you will be prompted for a driver. You should have received a suitable driver from esd for MS Windows operating systems (Windows 2000 and above).
Most Linux distributions bring their own driver for the used on-board FTDI USB-serial converter. When driver installation has been done you have a new virtual serial port (COMx on Windows and typically `/dev/ttyUSBx` on Linux). Now open a terminal program and point to the virtual COM port of the XMC-CPU/2041.
The default communication parameters are 9600 baud, 8N1 (8 data bits, no parity, 1 stopbit, no hardware handshake).

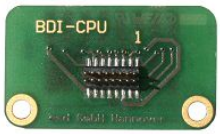
After the next power-on you will see the bootloader startup messages being output on the serial console. When you see the message 'Press SPACE ....', hit the space key to stop booting and to access the interactive bootloader console. At the prompt you can use an extensive command set to do configuration, debugging or testing tasks. Enter help (followed by hitting the RETURN key) to get a full list of all supported commands.

```
U-Boot 2011.12-00018-gaae5e2a-dirty (Feb 04 2014 - 12:30:11)

CPU0:  P2041, Version: 1.1, (0x82100111)
Core:  E500MC, Version: 2.2, (0x80230022) Clock Configuration:
       CPU0:1200 MHz, CPU1:1200 MHz, CPU2:1200 MHz, CPU3:1200 MHz,
       CCB:600  MHz,
       DDR:600  MHz (1200 MT/s data rate) (Asynchronous), LBC:75   MHz
       FMAN1: 500 MHz
       PME:   300 MHz
L1:    D-cache 32 kB enabled
       I-cache 32 kB enabled
Board: esd XMCP2041, 36-bit Addressing
Reset Configuration Word (RCW):
       00000000: 4c580000 00000000 18540000 00000000
       00000010: 149f90c0 c7c02000 58000000 40000000
       00000020: 00a00000 00000000 00000000 28078100
       00000030: 00000000 00000000 00000000 00000000
I2C:   ready
SPI:   ready
DRAM:  Initializing....using SPD
Detected UDIMM esd_cpu2041_512MB
DDR:   speed       1200
DDR:   512 MiB (DDR3, 64-bit, CL=9, ECC on) Testing 0x00000000 - 0x1fffffff Remap DDR
POST memory PASSED
L2:    128 KB enabled
Corenet Platform Cache: 1024 KB enabled
SERDES: timeout resetting bank 3
NAND:   nand_get_flash_type: unknown NAND device: Manufacturer ID: 0x8f, Chip ID: 0x8f
No NAND device found!!!
```

```
0 MiB
PCIe1: Root Complex, no link, regs @ 0xfe200000
PCIe1: Bus 00 - 00
PCIe2: Endpoint, x4, regs @ 0xfe201000
PCIE:  Unlock port
PCIE:  FSL_PCIE_CFG_RDY 00
PCIe2: Bus 01 - 01
PCIe3: Endpoint, x1, regs @ 0xfe202000
PCIE:  Unlock port
PCIE:  FSL_PCIE_CFG_RDY 00
PCIe3: Bus 02 - 02
In:    serial
Out:   serial
Err:   serial
Net:   Initializing Fman
Fman1: DTSEC4 set to RGMII
Fman1: DTSEC5 set to RGMII
Fman1: Uploading microcode version 101.8.0 PHY reset timed out PHY reset timed out PHY
reset timed out FM1@DTSEC1, FM1@DTSEC2, FM1@DTSEC3, FM1@DTSEC4 [PRIME], FM1@DTSEC5 Hit
any key to stop autoboot:  0 =>
```

8. Order Information

Type	Properties	Order No.
XMC-CPU/2041	Freescale PowerPC QorIQ P2041, 1.2 GHz Xilinx® FPGA Spartan® 6 XC6LXT-45T 2x Ethernet, 1x USB 2.0 62 LVTTL I/Os at connector PMC-P14	V.2029.01
Accessories		
XMC-CPU/2041-ADAPTER-BDI 	XMC-CPU/2041-ADAPTER-BDI Interface to connect the Abatron BDI2000 and BDI3000 to XMC-CPU/2014 X900 (Samtec CLM (16 pins) <-> box header (16 pins))	V.2029.02
XMC-CPU/2041-ADAPTER-NXP 	XMC-CPU/2041-ADAPTER-NXP Interface to NXP (Healthcontroller) XMC-CPU/2041 X900 (Samtec CLM (16 pin) <-> box header (6 pins))	V.2029.04
XMC-CPU/2041-ADAPTER-FPGA 	XMC-CPU/2041-ADAPTER-FPGA Interface to connect the Tool XILINX ChipScope to XMC-CPU/2041 X400 (Samtec CLM (8 pins) <-> box header (10 pins))	V.2029.03
Software		
XMC-CPU/2041-VxW	VxWorks BSP	V.2029.30
XMC-CPU/2041-Linux	Linux BSP	V.2029.32

For detailed information about the driver availability for your special operating system, please contact our sales team.

Table 13: Order information

PDF Manuals
Manuals are available in English and usually in German as well. For availability of English manuals see table below.
Please download the manuals as PDF documents from our esd website www.esd.eu for free.

Manuals		Order No.
XMC-CPU/2041-ME	Hardware manual in English	V.2029.21

Table 14: Available manuals

Printed Manuals
If you need a printout of the manual additionally, please contact our sales team: sales@esd.eu for a quotation. Printed manuals may be ordered for a fee.