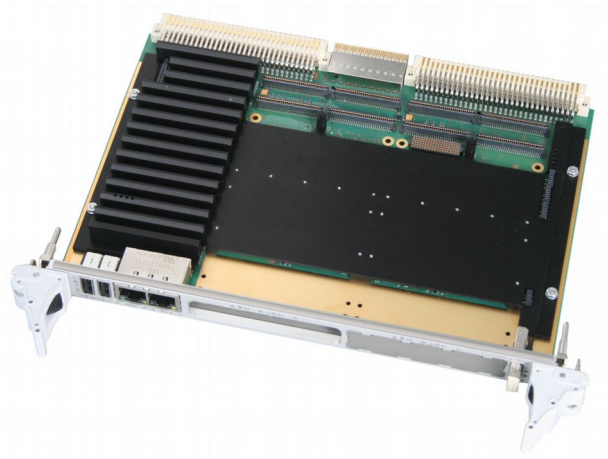
VME-PMC-CPU/2

Processor Board with 2 PMC Slots



Hardware Manual

to Products:

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	V.1917.14

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N O T E

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Document file:	I:\Texte\Doku\MANUALS\VME\PMC-CPU2\englisch\VME-PMC-CPU2_Hardware_en_12.odt
Date of print:	2015-08-12

Hardware version:	from Rev. 1.4

Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Revision	Chapter	Changes versus previous version	Date
1.1	7	Updated chapter 'Order Information' (new order no. for VME-PMC-CPU/2-CC CC + 32P2 → V.1917.14, removed VME-PMC-CPU/2 QNX BSP software driver)	2012-11-08
1.2	-	Safety Instructions and Informations revised	2015-08-12
	1.3.3, 3.2	Figures of -CC version new (coding switches are equipped on the bottom layer)	
	3.1	Figures new (coding switches are equipped on the bottom layer)	
	3.3	Text revised,description of SW100 inserted	
	3.4	new figure	
	3.5	new figure, default setting of contact 2 is OFF	

Technical details are subject to change without further notice.

Safety Instructions

- When working with VME-PMC-CPU/2 follow the instructions below and read the manual carefully to protect yourself from injury and the VME-PMC-CPU/2 from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- The device has to be securely installed in the control cabinet before commissioning.
- Protect the VME-PMC-CPU/2 from dust, moisture and steam.
- Protect the VME-PMC-CPU/2 from shocks and vibrations.
- The VME-PMC-CPU/2 may become warm during normal use. Always allow adequate ventilation around the VME-PMC-CPU/2 and use care when handling.
- Do not operate the VME-PMC-CPU/2 adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.
- Do not use damaged or defective cables to connect the VME-PMC-CPU/2 .
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The VME-PMC-CPU/2 may only be driven by power supply current circuits, that are contact protected. A power supply, that provides a safety extra-low voltage (SELV) according to EN 60950-1, complies with this conditions.

Danger!
Hazardous Voltage - Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the VME-PMC-CPU/2 is to be integrated. Disconnect all hazardous voltages (mains voltage) before opening the system.

Attention !
Electrostatic discharges may cause damage to electronic components.
To avoid this, please discharge the static electricity from your body *before* you touch the VME-PMC-CPU/2.

Qualified Personal
This documentation is directed exclusively towards personal qualified in control and automation engineering.
The installation and commissioning of the product may only be carried out by qualified personal, which is authorized to put devices, systems and electric circuits into operation according to the applicable national standards of safety engineering.

Conformity
The VME-PMC-CPU/2 is a sub-assembly intended for incorporation into an apparatus by a manufacturer and NOT by the end user. The manufacturer of the final system must decide, whether additional EMC or EMI protection requirements are necessary.

Data Safety
This device is equipped with an Ethernet or other interface which is suitable to establish a connection to data networks. Depending on the software used on the device, these interfaces may allow attackers to compromise normal function, get illegal access or cause damage.
esd does not take responsibility for any damage caused by the device if operated at any networks. It is the responsibility of the device's user to take care that necessary safety precautions for the device's network interface are in place.

Intended Use
The intended use of the VME-PMC-CPU/2 is the operation as as VME Processor Board with 2 PMC slots. .
The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.
- The VME-PMC-CPU/2 is intended for installation in VMEbus systems only.
- The operation of the VME-PMC-CPU/2 in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the VME-PMC-CPU/2 for medical purposes is prohibited.

Service Note
The VME-PMC-CPU/2 does not contain any parts that require maintenance by the user. The VME-PMC-CPU/2 does not require any manual configuration of the hardware except the coding switch setting (see from page 20). Unauthorized intervention in the device voids warranty claims.

Disposal
Devices which have become defective in the long run have to be disposed in an appropriate way or have to be returned to the manufacturer for proper disposal. Please, make a contribution to environmental protection.

Content

1. Overview

1.1 Description of VME-PMC-CPU/2

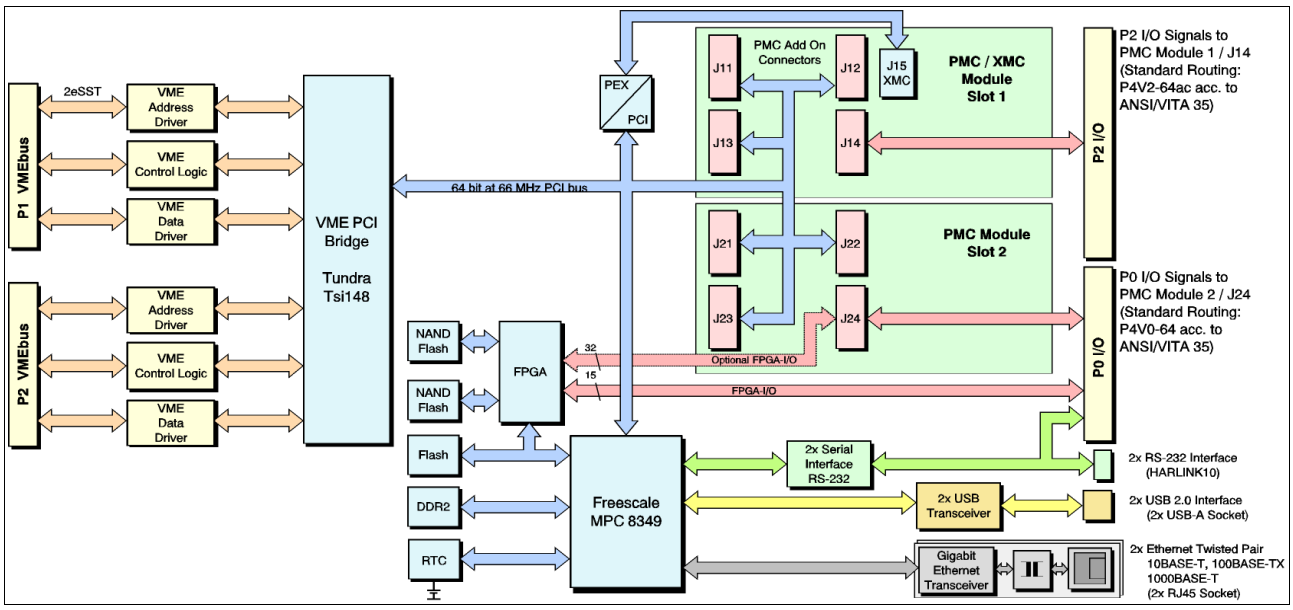


Fig. 1: Block circuit diagram of VME-PMC-CPU/2 (V.1917.01, V.1917.02)

1.2 General

The VME-PMC-CPU/2 is a VME64-base board which can carry up to two PMC modules of normal size. For the VMEbus connection the VME-PCI bridge Tsi148 by Tundra is used.

The Tsi148 is designed in a way that the board can either operate as slave or as master on the VMEbus. If the board operates as master, it supports a 4-level arbiter. The VMEbus interrupt can be applied to any of the seven interrupt-request lines. The first green LED signal indicates VMEbus interrupt requests. The second green LED, which is located in the front panel, is active during VMEbus access (not available for Conduction Cooled version). The VME-PMC-CPU/2 is connected to the VMEbus by two 160-pin VG-connectors (acc. to DIN 41612) for VME64 systems and one 95-pin I/O-connector (acc. to IEC 1076-4-101).
Both PMC slots are designed according to the standard IEEE Std 1386-2001 (except the standard I/O pin routing). The slots are also designed for PPMC modules according to VITA32™. Slot 1 has an XMC connector according to VITA42.3.
PMC modules, that use 3.3 V signalling only, can be used.
In addition to the connectors for the PMC address/data and control signals, every slot of the VME-PMC-CPU/2 has an I/O-connector which applies the I/O-signals of the PMC modules to VMEbus connectors P2 and P0.
The VME-PMC-CPU/2 is equipped with 2 USB-host interfaces (USB2.0) and 2 Ethernet interfaces (IEEE802.3), which are accessible via front panel.
The front panel of the VME-PMC-CPU/2 has two cutouts for the front panels of the PMC modules. A blank cover for unused slots is included in the scope of delivery.

Example libraries for the initialization of the board in C source code for VxWorks® are available for a fee. Drivers for other operating systems are available on request. Please state your operating system with the version number when you order.

1.3 Characteristics of the Available Hardware Options

Note:
All options given below have to be specified when ordering. They can not be installed later. For an overview of the possible combinations of the options see page 49.

1.3.1 Option “-32P2”: Changed I/O-Pin Routing on P2

The VME-PMC-CPU/2 is currently available with two different I/O-pin assignments:

- In the standard configuration each of the I/O-pins of the PMC slot 1 (J14) is connected to exactly one pin of the VMEbus connector P2 (according to VITA 35 (P4V2-64ac)) and each of the I/O-pins of the PMC slot 2 (J24) is connected with exactly one I/O-pin of the VMEbus connector P0 (according to VITA 35 (P4V0-64)).

- In the VME-PMC-CPU/2 with the option '-32P2' the pins are assigned according to IEEE Std.1386-2001, Table 8. In this option the I/O-signals of both PMC slots are connected with the pin rows a+c of the VME connector P2:
  The pins 33...64 of the PMC connector J24 are connected in parallel to this also to the rows a and c of the P2 connector. This causes a double assignment of the pins a1..a16 and c1...c16 on P2. Furthermore by this both PMC slots are connected with each other via 32 of their I/O-pins.

Note:
The advantage of this solution is the access via one standard VMEbus P2-I/O adapter to each the half of the I/O-signals of both PMC slots.

Attention!
You have to pay attention that your choice of inserted PMC modules does not lead to undesired interactions between the modules, due to the I/O-signal connection between the slots!

1.3.2 Option “-T”: Extended Temperature Range

The VME-PMC-CPU/2 with this option is designed for the operation in the extended temperature range of -40 °C ...+75 °C.

1.3.3 Option: “-CC”: Conduction Cooled

The VME-PMC-CPU/2-CC is designed with covering heat sinks for heat dissipation in conduction cooled systems. The slots of the PMC modules are designed to carry conduction cooled PMC modules.

As a result of the heat sinks the front panel and with it the 10-pin har-link-connector with the serial interfaces are not equipped. Furthermore the front panel LEDs are not equipped.

The conduction cooled version VME-PMC-CPU/2 is designed for operation in the extended temperature range from -40 °C ...+75 °C as the VME-PMC-CPU/2-T version.

Fig. 2: Conduction cooled version VME-PMC-CPU/2-CC

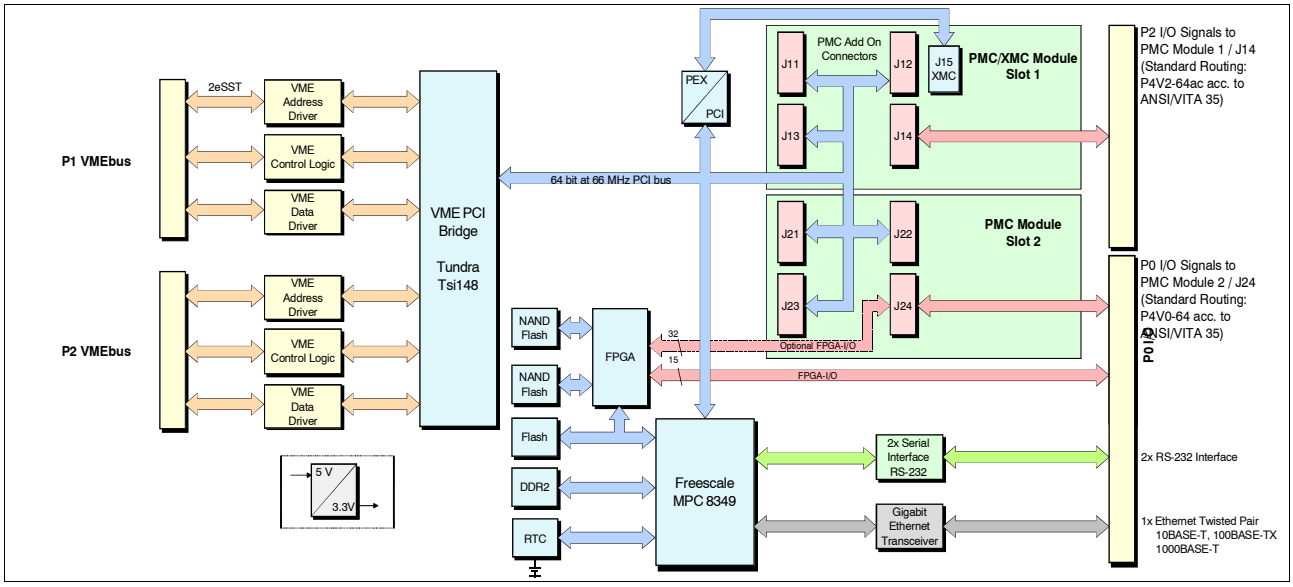


Fig. 3: Block circuit diagram of VME-PMC-CPU/2-CC (V.1917.03)

1.4 Technical Data

1.4.1 General Technical Data

VMEbus interface	IEEE 1014 / Rev. D Master or Slave functionality
Base address	geographical addressing
Address modifier	standard supervisory and non-privileged data access, extended supervisory and non-privileged data access, short supervisory and non-privileged access
VMEbus access	- Legacy-protocols supporting the preservation of existing VMEbus systems - VME64 extensions - 2eVME- and 2eSST protocols
VMEbus back plane	compatible to VME32, VME64 and VME64x back planes
Ambient temperature range	Standard: 0...50 °C (order no.: V.1917.01/.11) Extended temperature range: -40...+75 °C (order no.: V.1917.02 /.13) Conduction cooled: -40...+75 °C (order no.: V.1917.03)
Humidity	max. 90%, non-condensing
Connectors	P1, P2 - 160-pin VG-connector according to DIN 41612 in compliance with VME64 extension P0 - 95-pin I/O-connector according to IEC 1076-4-101
	<u>J11 to J24 - 64-pin PMC socket connectors:</u> J11, J12, J21, J22 - PMC address/data signals J13, J23 - PCI (64 signals) J14, J24 - PMC I/O-signals J15 - 114-pin XMC socket
	X1400 - 2x RJ45: IEEE802.3 Ethernet Port 1+2
	X1630 - USB-A-socket: USB Port 1 X1720 - USB-A-socket: USB Port 2
	X1940 - 10-pin har-link socket: 2x serial (RS-232) (not at VME-PMC-CPU/2)
	<u>Service- and diagnostic connectors:</u> X1800 - socket connector 1x16: Debug CPU X1801 - socket connector 1x7: JTAG-TSI148 X2120 - socket connector 1x7: JTAG-PCI X2310 - socket connector 1x6: ISP-ADUC848 X2700 - socket connector 1x7: JTAG-FPGA
Dimensions	160 mm x 233 mm
Slot format	6 U high / 4 HP wide
Weight	VME-PMC-CPU/2 (order no.: V.1917.01/.02/.11/.13): ca. 610 g VME-PMC-CPU/2-CC (order no.: V.1917.03): ca. 650 g
Power supply voltage (without PMC modules)	VMEbus P1, P2: 5 V ±5% / ca. 1.8 A 3.3 V not in use (see chapter. 1.4.7) +12V ±5% ((only to PMC slots) -12V ±5% ((only to PMC slots)

Table 1: General technical data

1.4.2 Microprocessor and Memory

CPU	Freescale MPC 8349
Clock rate	Standard: 533 MHz Optional: 667 MHz (only available for order no.: V.1917.01/.11)
NOR-Flash	128 MByte Flash
NAND-Flash-EPROM	2 GByte
RAM	512 MByte DDR2 RAM ECC

Table 2: Microprocessor and memory

1.4.3 Real-time Clock

Function	Time and calendar (RTC RX8025SA)
Backup	High Temperature Supercapacitor C = 0,85 F

Table 3: Real-time clock

1.4.4 Serial Interfaces

Number	2
Controller	UART in MPC8349
Signals	to X1940: RxD, TxD, RTS, CTS (for each port) to VMEbus P0: RxD, TxD (for each port)
Bit rate	300 bit/s ... 115.200 bit/s
Physical interface	RS-232
Connector	X1940 (10-pin har-link) and VMEbus P0, Adapter cable 10-pol har-link to 9-pin DSUB available

Table 4: Serial interfaces

1.4.5 ETHERNET-Interfaces

Number	2, only one in CC-version
Bit rate	10 Mbit/s, 100 Mbit/s, 1000 Mbit/s
Controller	MPC8349
Physical interface	Twisted Pair (IEEE802.3)
Galvanic isolation	via transmitters
Connector	8-pin RJ45-socket with LEDs in the front panel.

Table 5: ETHERNET-Interfaces

1.4.6 USB Host Interfaces

Number	2 (not available in CC-version)
Interface	USB 2.0, host, high speed, 480 Mbit/s
Controller	Integrated in MPC8349
Connector	USB1: X1620, 4-pin USB-A-socket USB2: X1720, 4-pin USB-A-socket

Table 6: USB host interfaces

1.4.7 PMC Slots

PMC standard	IEEE Std 1386-2001, IEEE Std 1386.1-2001
Equipment	two single-size modules
VME-PCI-Bridge	Tundra Tsi148
I/O-Signals to VMEbus P2 and P0	Standard: according to VITA 35 (P4V2-64ac, P4V0-46), i.e. PMC slot 1 (J14) completely to P2 row a and c, PMC slot 2 (J24) completely to VMEbus connector P0 Option '-32P2': PMC slot 1 (J14): as above but additionally on P2 parallel assignment with J24 pins 33...64, PMC slot 2 (J24): as above but additionally on P0 parallel assignment with J14-pins 1...32
Signal voltage level	3.3V **Attention!** If the 3.3V-supply of the whole VME-PMC-CPU/2 should be generated directly from the supply of the VMEbus, you have to remove the SMD-resistors RX2530 and RX2535 first!*
Power supply voltage	3.3V: The 3.3V supply voltage of the PMC modules is generated from the +5V-supply of the VMEbus. A single PMC slot has a max. current consumption of 1.5 A. 3.3V AUX: max. 250 mA current consumption for both PMC slots together +12V: max. 1.0 A current consumption per PMC slot -12V: max. 1.0 A current consumption per PMC slot

* At the moment this hardware option has no specific order no.. If you would like to order the VME-PMC-CPU/2 with this option, please contact our sales team (sales@esd.eu) before ordering.

Note:
The maximum permissible power consumption of one PMC module of 15 W for double-sided modules is defined in the IEEE Std. 1386-2001.

Table 7: PMC Slots

1.4.8 XMC Slots

XMC standard	VITA 42.3, Link-definition according to table 4-1: Single width, 4-Lane, only connector P15 is used.
Bus system	PCI-EXPRESS®
Connector	Connector assignment according to VITA 42.3, table 4-2
Power supply	U_{VPWR} = 5V ±5 % (max. 1.0 A current consumption) ((alternatively, adjustable via solder bridges U_{VPWR} = 12V ±5%) * $U_{3.3V}$ = 3.3 V ±0,3V (max. 1.0 A current consumption) $U_{3.3VAUX}$ = 3.3 V ±0,3V (max. 1.0 A current consumption) U_{+12V} = +12 V ±5 % (max. 1.0 A current consumption) U_{-12V} = -12 V ±5 % (max. 1.0 A current consumption) **Note:** The maximum permissible power consumption of one PMC module of 15 W for double-sided modules is defined in the IEEE Std. 1386-2001.

* At the moment this hardware option has no specific order no.. If you would like to order the VME-PMC-CPU/2 with this option, please contact our sales team (sales@esd.eu) before ordering.

Table 8: XMC Slots

1.4.9 Software

Board Support Packages (BSPs) are available for VxWorks 5.5 and VxWorks 6.7. Moreover esd offers BSPs for Linux® and QNX® . If you need this hardware variant, please contact our sales team (sales@esd.eu) before ordering.

2. Front Panel and LEDs

2.1 VME-PMC-CPU/2

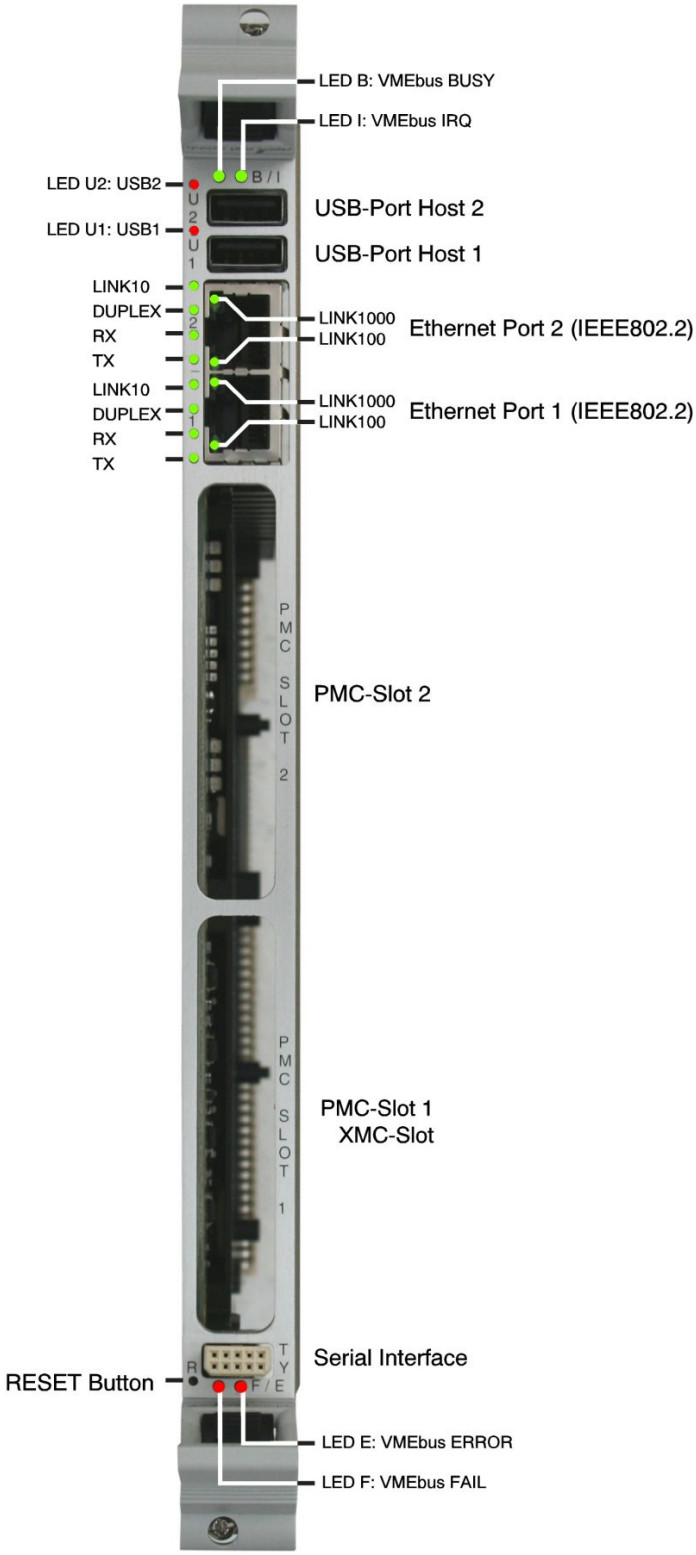


Fig. 4: Front of the VME-PMC-CPU/2

2.2 VME-PMC-CPU/2-CC

Fig. 5: Front of the conduction cooled version VME-PMC-CPU/2-CC

2.3 Declaration of the LEDs

2.3.1 Front panel LEDs

2.3.1.1 VMEbus LEDs (only for VME-PMC-CPU/2)

LED			Meaning (LED on)
Labelling on front panel	Name	Colour	
B	BUSY	green	Access from VMEbus to VME-PMC-CPU/2
I	IRQ	green	VME-PMC-CPU/2 triggers an interrupt on the VMEbus
F	FAIL	red	VME-PMC-CPU/2 triggers FAIL on VMEbus
E	BERR	red	VME-PMC-CPU/2 triggers Bus-Error on VMEbus

Table 9: Indication of the VMEbus LEDs

2.3.1.2 USB LEDs (only for VME-PMC-CPU/2)

LED			Meaning (LED on)
Labelling on front panel	Name	Colour	
U1	USB-Power 1	red	USB-power at port 1 is active
1)*	LED1710 (MPH_PCLT0)	red	USB-port1-status-indicator bit 0
1)*	LED1711 (MPH_PCLT1)	red	USB-port1-status-indicator bit 1
U2	USB-Power 2	red	USB-power at port 2 is active
1)*	LED1610 (MPH_PCLT0)	red	USB-port2-status-indicator bit 0
1)*	LED1611 (MPH_PCLT1)	red	USB-port2-status-indicator bit 1

Table 10: Indication of the USB-LEDs

1)* These LEDs have no function in the CC-version.

2.3.1.3 Ethernet LEDs

LED			Meaning (LED on)
Labelling on front panel	Name	Colour	
Left LED of a socket	LINK1000	green	Link status Ethernet 1Gbit/s (connection to switch or hub resp. available)
Right LED of a socket	LINK100	green	Link status Ethernet 100 kbit/s (connection to switch or hub resp. available)
2	LINK10	green	Link status Ethernet 10 kbit/s
	DUPLEX	green	Full duplex mode (LED off: half duplex mode)
	RX	green	Receive traffic at Ethernet-port 2
	TX	green	Transmit traffic at Ethernet-port 2
1	LINK10	green	Link status Ethernet 10 kbit/s
	green	green	Full duplex mode (LED off: Half duplex mode)
	RX	green	Receive traffic at Ethernet-port 1
	TX	green	Transmit traffic at Ethernet-port 1

Table 11: Indication of the Ethernet LEDs of the Ethernet-LEDs

The position of the LEDs is described at Fig. 6 on page 15, resp. Fig. 7 on page 16 (conduction cooled version).

2.3.1.4 PCI EXPRESS LEDs

These LEDs indicate the status of the PCI-EXPRESS bridge for XMC- J15.

LED			Meaning (LED on)
Labelling on front pane	Name	Colour	
*	PEX_LG0	red	PCI-EXPRESS lane 0 is active
*	PEX_LG1	red	PCI-EXPRESS lane 1 is active
*	PEX_LG2	red	PCI-EXPRESS lane 2 is active
*	PEX_LG3	red	PCI-EXPRESS lane 3 is active

Table 12: Indication of the PCI EXPRESS-LEDs

* This LED is not located in the front panel. The position of the LED is described at Fig. 6 on page 20, resp. Fig. 7 on page 22 (conduction cooled version).

2.4 Reset Button

The reset can be enabled by pushing with a non-conducting bar-shaped object (<1.5 mm diameter).
A local reset at the VME-PMC-CPU/2 and consequently at on the PMC modules is triggered. If the CPU is configured as system controller, a reset is triggered at the VMEbus, too.

3. PCB View with Coding Switches and Connectors

3.1 VME-PMC-CPU/2

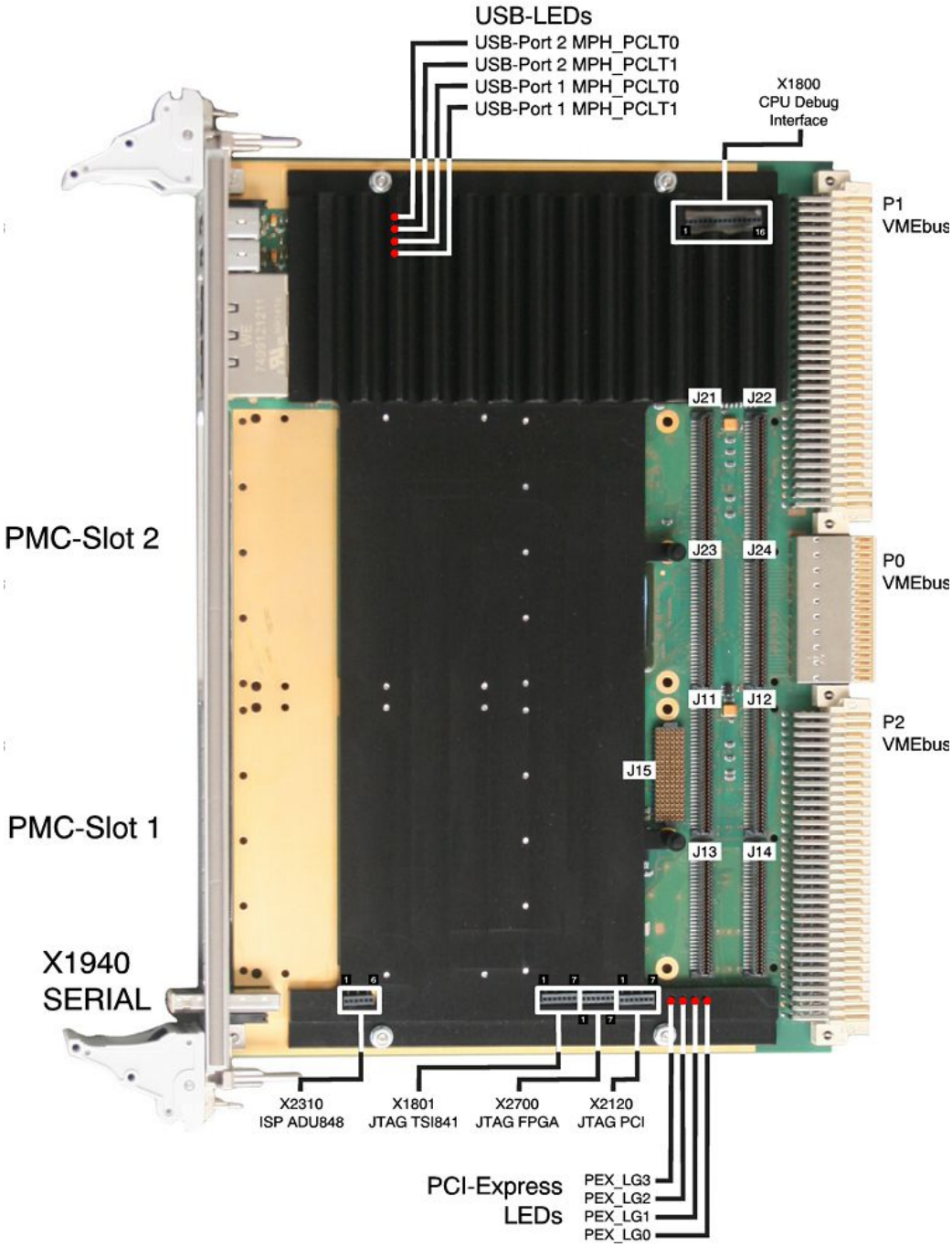


Fig. 6: Top layer view of VME-PMC-CPU/2

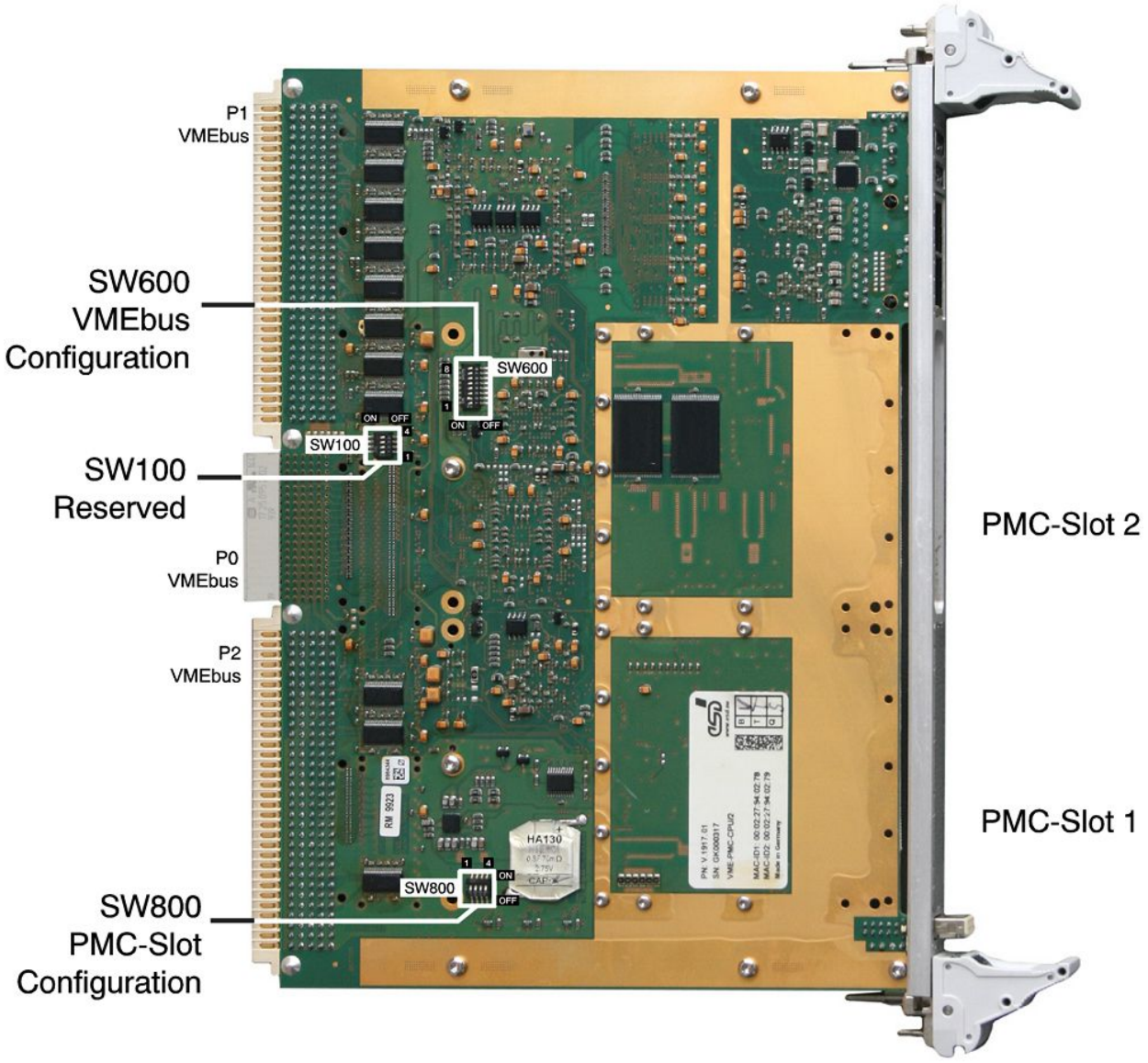


Fig. 7: Bottom layer view with coding switches of VME-PMC-CPU/2

3.2 VME-PMC-CPU/2-CC

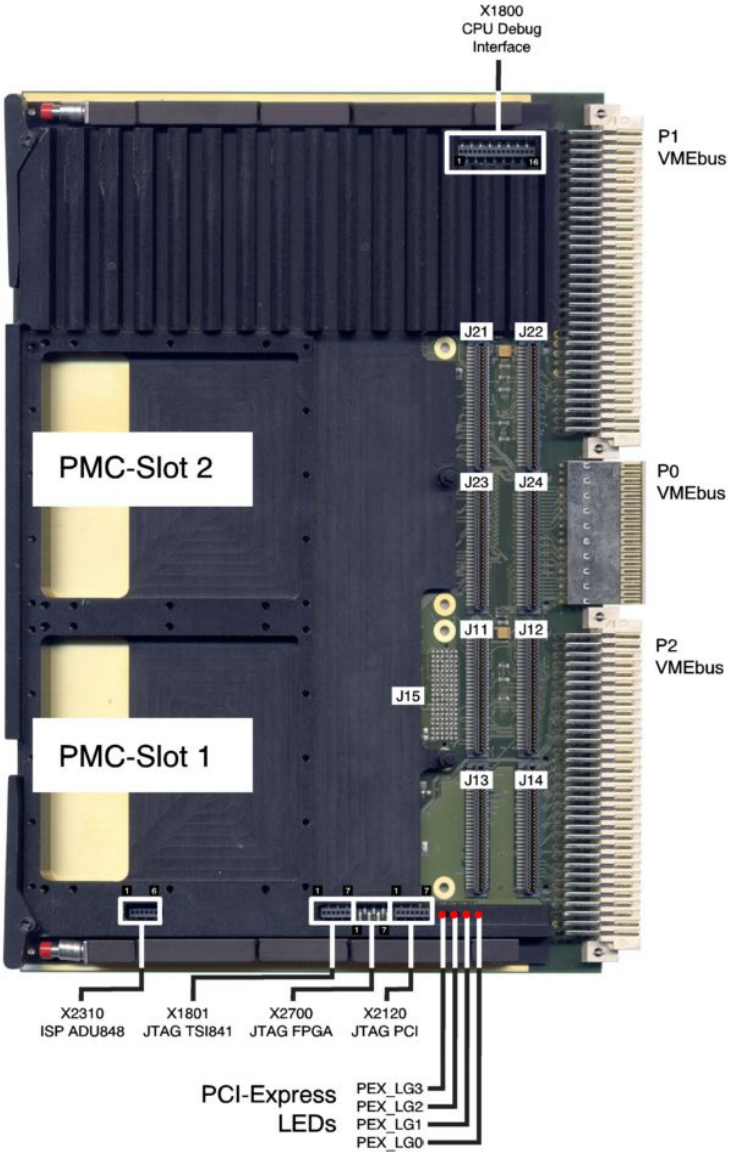


Fig. 8: Position of the connectors at VME-PMC-CPU/2-CC

Note:
The position of the coding switches SW800, SW600, SW100 of the VME-PMC-CPU/2-CC is the same as described for the of the VME-PMC-CPU/2, see Figure 7 on page 21.

3.3 Default Setting of the Coding Switches

The default settings of the board are shown in the following table. The coding switches are equipped on the bottom layer of the VME-PMC-CPU/2. The position of the coding switch is shown in Fig. 7 on page 21. In the following descriptions the coding switches are shown as if the board is viewed with the VMEbus connectors on the left (view from PMC slot side).

Coding Switch		Setting	Value	Description	
SW600	8	OFF	1	SFAILEN Control Bit Reset Value	VMEbus Power Up Options
	7	OFF	1	SFAILAI Control Bit Auto Clear	
	6	ON	0	Auto Slot ID Enable	
	5	ON	0	Geographical Slot ID Enable	
	4	OFF	1	not used	
	3	OFF	1	not used	
	2	OFF	1	VMEbus System Controller: Default: System Controller function disabled	
	1	ON	0		
SW800	4	OFF	1	PMC module 1 is not configured as Monarch	
	3	OFF	1	PMC module 2 is not configured as Monarch	
	2	OFF	1	PCI-Bus of the PMC module is set to the fixed value of 66 MHz	
	1	OFF	1	(PUPEN) reserved for future applications	
SW100	4	OFF	1	reserved	
	3	OFF	1		
	2	OFF	1		
	1	OFF	1		

Table 13: Overview of the default settings of the coding switches

Note:
The default position of the contacts of coding switch SW100 is OFF.
Do not change the settings!

3.4 VMEbus Configuration (SW600)

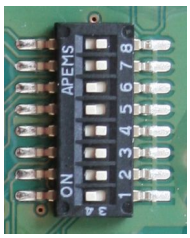


Fig. 9: Coding Switch SW600

3.4.1 Overview

Coding Switch Contact	Bit Name	Function	Default Setting
8	SFAILEN Control Bit Reset Value	VMEbus Power-Up Options	OFF
7	SFAILAI Control Bit Auto Clear		OFF
6	Auto Slot ID Enable		ON
5	Geographical Slot ID Enable		ON
4	not used	these coding switches are not evaluated	OFF
3	not used		OFF
2	SCONEN#	VMEbus System Controller setup	OFF
1	SCONDIS#		ON

Table 14: Assignment of the coding switch SW600

Value of the parameter bits:

ON: Bit = ‘0’

OFF: Bit = ‘1’

3.4.2 VMEbus System Controller Setup

These bits define how and whether the VME-PMC-CPU/2 is configured as VMEbus System Controller.

Coding switch contact 2	Coding switch contact 1	Function
SCONEN#	SCONDIS#	
OFF	OFF	Auto SCON: automatic enabling of the System Controller (depending of signal VBG3IN#)
ON	OFF	System Controller disabled
OFF	ON	System Controller disabled
ON	ON	not allowed

Table 15: VMEbus System Controller activation

Value of the parameter bits:

ON: Bit = ‘0’

OFF: Bit = ‘1’

3.4.3 VMEbus Power-Up Options

After a reset the Tundra PCI/X-to-VMEbus-bridge TS148 evaluates different PCI/X-bus and VMEbus signals to enable or disable various functions. For the VMEbus the data signals VD[0] to VD[3] are evaluated.

Coding switch contact	VMEbus data bit	Power-up option	Description
8	VD[0]	SFAILEN_RV	SFAILEN Control Bit Reset Value
7	VD[1]	SFAILAI_AC	SFAILAI Control Bit Auto Clear
5	VD[2]	ASIDEN	Auto Slot ID Enable
6	VD[3]	GSIDEN	Geographical Slot ID Enable

Table 16: VMEbus-Power-Up option bits

Note:
Please, refer to chapter '5.4.2 VMEbus Power-up Options' in the manual of the Tundra PCI/X-to-VMEbus-Bridge TS148 [1] for details about the comprehensive VMEbus Power-Up options.

3.5 PMC Slot Configuration (SW800)

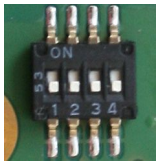


Fig. 10: Coding switch SW800

Coding switch contact	Name	Description	Default
4	P-MONARCH 1#	Monarch/Non-Monarch PMC module 1 OFF: Non-Monarch ON: Monarch (PPMC)	OFF
3	P-MONARCH 2#	Monarch/Non-Monarch PMC module 2 OFF: Non-Monarch ON: Monarch (PPMC)	OFF
2	P-M66EN	Clock rate of the PCI-Bus of the PMC modules: OFF: 66 MHz ON: 33 MHz	OFF
1	P-PUPEN	reserved for future applications; always set to 'OFF'	OFF

Table 17: PMC slot configuration via SW800

4. Address Assignment of the VME-PMC-CPU/2

Address range	Assignment
0x00000000 ... 0x1fffffff	DDR2 RAM (72 bit data width)
0x80000000 ... 0x8fffffff	PCI Memory Space (prefetchable)
0x90000000 ... 0x9fffffff	PCI Memory Space
0xe0000000 ... 0xe00fffff	CPU IMMR
0xe2000000 ... 0xe20fffff	PCI IO Space
0xf0000000 ... 0xf003ffff	Local Bus to FPGA
0xf8000000 ... 0xffffffff	FLASH (16 bit data width)

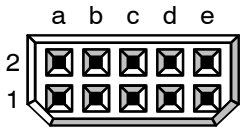
Table 18: Address assignment

5. Connector Assignment

5.1 Serial Interface RS-232 (X1940)

Socket: har-link® female multipoint connector 10-pin., Harting No.: 27211218000

Pin-Position:



Pin-Assignment:

Pin	Signal	
	Row 1	**Row 2**
a	TXS1	RXS1
b	RTSS1#	CTSS1#
c	TXS2	RXS2
d	RTSS2#	CTSS2#
e	GND	+5V
z	Shield	Shield

Signal Description:

TXSx, RXSx, RTSSx#, CTSSx# ... Control signal data of the serial interface 1 and 2 (x = 1, 2). The signal starts at VME-PMC-CPU/2 (i.e. TXSx = Output)

> **Attention!**
> The signals TXS1, RXS1, TXS2 and RXS2 are additionally routed to VMEbus P0 (See page 41).

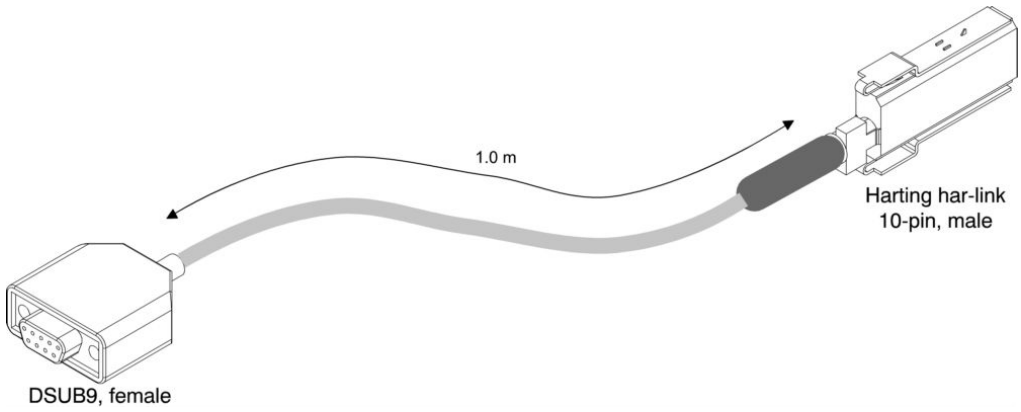
GND ... reference potential of the serial interface

+5V ... power supply, connected to +5V of the VMEbus, max. allowed charge I_{Load} < 100 mA

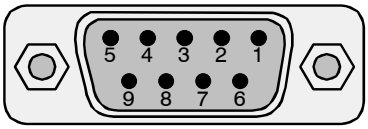
Shield ... contact to enclosure shield of the har-link-socket: Shield is connected to the front panel of the VME-PMC-CPU/2

5.2 Adapter Cable 'VME-PMC-CPU/Cable'

An adapter cable from 10-pin har-link to 9-pin DSUB (order no.: V.1917.25) is available for the connection of the serial interface 1.



Pin Position DSUB9:



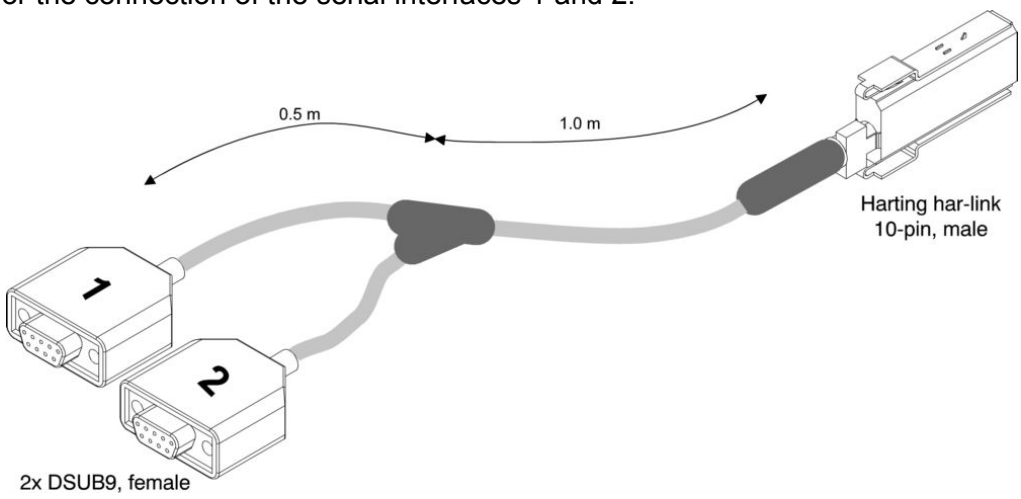
Pin Assignment:

DSUB9		Signal direction *	har-link
Pin	**Signal**		**Pin**
1	-		-
2	TXS1	←	a1
3	RXS1	→	a2
4	-		-
5	GND		e1
6	-		-
7	CTSS1#	→	b2
8	RTSS1#	←	b1
9	-		-
-	Shield		Shield

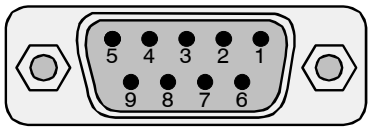
* The signal direction is described as seen from the VME-PMC-CPU/2.
-... This pin is not connected.
See page 30 for signal description.

5.3 Adapter Cable 'VME-PMC-CPU/Cable-Y'

An adapter cable with Y-junction from 10-pin har-link to 2x 9-pin DSUB (order no.: V.1917.26) is available for the connection of the serial interfaces 1 and 2.



Pin Position DSUB9:



Pin Assignment:

DSUB9 "1"		Signal direction *	har-link
Pin	Signal		Pin
1	-		-
2	TXS1	←	a1
3	RXS1	→	a2
4	-		-
5	GND		e1
6	-		-
7	CTSS1#	→	b2
8	RTSS1#	←	b1
9	-		-
-	Shield		Shield

DSUB9 "2"		Signal direction *	har-link
Pin	Signal		Pin
1	-		-
2	TXS2	←	c1
3	RXS2	→	c2
4	-		-
5	GND		e1
6	-		-
7	CTSS2#	→	d2
8	RTSS2#	←	d1
9	-		-
-	Shield		Shield

* The signal direction is described as seen from the VME-PMC-CPU/2.
-... This pin is not connected.
See page 30 for signal description.

5.4 USB (X1620, X1720)

Both USB-host interfaces are equipped with type A-sockets. Design and pin assignment is according to the USB-Serial Bus Specification 2.0.
The current consumption of connected USB-hardware is limited to 500 mA per USB-socket.

5.5 Ethernet IEEE 802.3

5.5.1 VME-PMC-CPU/2 (X1400A+B)

The Ethernet interfaces are equipped with 8-pin RJ45-sockets (8P8C) according to TIA-568A/B.

5.5.2 VME-PMC-CPU/2-CC (P0)

The signals of the Ethernet interface 1 of the VME-PMC-CPU/2-CC (Conduction Cooled) are accessible via VMEbus connector P0 (see page 41). An adapter is required. The adapter is optionally equipped with a transmitter.

5.6 Recommended Cable Types

To ensure the functionality of networks with bit rates up to 1-GBit/s, only CAT5e cables or better should be used.

5.7 VMEbus P1

Pin	Row z	Row a	Row b	Row c	Row d	Pin
1	-	D00	BBSY*	D08	-	1
2	GND	D01	BCLR*	D09	GND	2
3	-	D02	ACFAIL*	D10	-	3
4	GND	D02	BG0IN*	D11	-	4
5	-	D04	BG0OUT*	D12	-	5
6	GND	D05	BG1IN*	D13	-	6
7	-	D06	BG1OUT*	D14	-	7
8	GND	D07	BG2IN*	D15	-	8
9	-	GND	BG2OUT*	GND	GAP*	9
10	GND	SYSCLK	BG3IN*	SYSFAIL*	GA0*	10
11	-	GND	BG3OUT*	BERR*	GA1*	11
12	GND	DS1*	BR0*	SYSRESET*	+3.3V	12
13	-	DS0*	BR1*	LWORD*	GA2*	13
14	GND	WRITE*	BR2*	AM5	+3.3V	14
15	-	GND	BR3*	A23	GA3*	15
16	GND	DTACK*	AM0	A22	+3.3V	16
17	-	GND	AM1	A21	GA4*	17
18	GND	AS*	AM2	A20	+3.3V	18
19	-	GND	AM3	A19	-	19
20	GND	IACK*	GND	A18	+3.3V	20
21	-	IACKIN*	-	A17	-	21
22	GND	IACKOUT*	-	A16	+3.3V	22
23	-	AM4	GND	A15	-	23
24	GND	A07	IRQ7*	A14	+3.3V	24
25	-	A06	IRQ6*	A13	-	25
26	GND	A05	IRQ5*	A12	+3.3V	26
27	-	A04	IRQ4*	A11	-	27
28	GND	A03	IRQ3*	A10	+3.3V	28
29	-	A02	IRQ2*	A09	-	29
30	GND	A01	IRQ1*	A08	+3.3V	30
31	-	-12 V	+5V STBY	+12 V	GND	31
32	GND	+5 V	+5 V	+5 V	-	32

160-pin VG-connector according to DIN41612
I_{max} per pin : 1.0 A
- ... Signal is not connected on the board

5.8 Standard Assignment of I/O-Signals

5.8.1 Standard Assignment VMEbus P2 (According to VITA 35, P4 V2-64ac)

In the standard assignment the I/O signals of the PMC slot 1 (J14) are connected to the rows a+c.

Pin	Row z	Row a	Row b	Row c	Row d	Pin
1	-	I/O102	+5 V	I/O101	-	1
2	GND	I/O104	GND	I/O103	-	2
3	-	I/O106	BRETRY*	I/O105	-	3
4	GND	I/O108	A24	I/O107	-	4
5	-	I/O110	A25	I/O109	-	5
6	GND	I/O112	A26	I/O111	-	6
7	-	I/O114	A27	I/O113	-	7
8	GND	I/O116	A28	I/O115	-	8
9	-	I/O118	A29	I/O117	-	9
10	GND	I/O120	A30	I/O119	-	10
11	-	I/O122	A31	I/O121	-	11
12	GND	I/O124	GND	I/O123	-	12
13	-	I/O126	+5 V	I/O125	-	13
14	GND	I/O128	D16	I/O127	-	14
15	-	I/O130	D17	I/O129	-	15
16	GND	I/O132	D18	I/O131	-	16
17	-	I/O134	D19	I/O133	-	17
18	GND	I/O136	D20	I/O135	-	18
19	-	I/O138	D21	I/O137	-	19
20	GND	I/O140	D22	I/O139	-	20
21	-	I/O142	D23	I/O141	-	21
22	GND	I/O144	GND	I/O143	-	22
23	-	I/O146	D24	I/O145	-	23
24	GND	I/O148	D25	I/O147	-	24
25	-	I/O150	D26	I/O149	-	25
26	GND	I/O152	D27	I/O151	-	26
27	-	I/O154	D28	I/O153	-	27
28	GND	I/O156	D29	I/O155	-	28
29	-	I/O158	D30	I/O157	-	29
30	GND	I/O160	D31	I/O159	-	30
31	-	I/O162	GND	I/O161	GND	31
32	GND	I/O164	+5 V	I/O163	-	32

160-pin VG-connector according to DIN41612
I_{max} per pin : 1.0 A
- ... Signal is not connected on the board

5.8.2 Standard Assignment of Transfer Module with P2 Row a and c Signals

The table below shows the assignment of a 64-pole transfer module connected to P2 connector. The 64 contacts of the module are connected to the signals of the rows a and c of the connector P2. Thus all I/O-contacts of the PMC slot 1 (J14) are accessible via the transfer module.

Assignment of a 64-pin transfer module					
Pin	Assignment of the I/O connector P2				Pin
	Row a	Signal		Row c	
2	1	I/O102	I/O101	1	1
4	2	I/O104	I/O103	2	3
6	3	I/O106	I/O105	3	5
8	4	I/O108	I/O107	4	7
10	5	I/O110	I/O109	5	9
12	6	I/O112	I/O111	6	11
14	7	I/O114	I/O113	7	13
16	8	I/O116	I/O115	8	15
18	9	I/O118	I/O117	9	17
20	10	I/O120	I/O119	10	19
22	11	I/O122	I/O121	11	21
24	12	I/O124	I/O123	12	23
26	13	I/O126	I/O125	13	25
28	14	I/O128	I/O127	14	27
30	15	I/O130	I/O129	15	29
32	16	I/O132	I/O131	16	31
34	17	I/O134	I/O133	17	33
36	18	I/O136	I/O135	18	35
38	19	I/O138	I/O137	19	37
40	20	I/O140	I/O139	20	39
42	21	I/O142	I/O141	21	41
44	22	I/O144	I/O143	22	43
46	23	I/O146	I/O145	23	45
48	24	I/O148	I/O147	24	47
50	25	I/O150	I/O149	25	49
52	26	I/O152	I/O151	26	51
54	27	I/O154	I/O153	27	53
56	28	I/O156	I/O155	28	55
58	29	I/O158	I/O157	29	57
60	30	I/O160	I/O159	30	59
62	31	I/O162	I/O161	31	61
64	32	I/O164	I/O163	32	63

5.8.3 Standard Assignment VMEbus P0

Pin	Row f	Row e	Row d	Row c	Row b	Row a
1	GND	(ETH1_MDI2_P)	(ETH1_MDI2_N)	GND	(ETH1_MDI0_N)	(ETH1_MDI0_P)
2	GND	(ETH1_MDI1_P)	(ETH1_MDI1_N)	GND	(ETH1_MDI3_N)	(ETH1_MDI3_P)
3	GND	RXS2	TXS2	RXS1	TXS1	GND
4	GND	I/O201	I/O202	I/O203	I/O204	I/O205
5	GND	I/O206	I/O207	I/O208	I/O209	I/O210
6	GND	I/O211	I/O212	I/O213	I/O214	I/O215
7	GND	I/O216	I/O217	I/O218	I/O219	I/O220
8	GND	I/O221	I/O222	I/O223	I/O224	I/O225
9	GND	FPGA-XI/O41	FPGA-XI/O42	FPGA-XI/O43	FPGA-XI/O46	FPGA-XI/O47
10	GND	FPGA-XI/O38	FPGA-XI/O39	FPGA-XI/O40	FPGA-XI/O44	FPGA-XI/O45
11	GND	FPGA-XI/O35	FPGA-XI/O36	FPGA-XI/O37	FPGA-XI/O34	FPGA-XI/O33
12	GND	I/O226	I/O227	I/O228	I/O229	I/O230
13	GND	I/O231	I/O232	I/O233	I/O234	I/O235
14	GND	I/O236	I/O237	I/O238	I/O239	I/O240
15	GND	I/O241	I/O242	I/O243	I/O244	I/O245
16	GND	I/O246	I/O247	I/O248	I/O249	I/O250
17	GND	I/O251	I/O252	I/O253	I/O254	I/O255
18	GND	I/O256	I/O257	I/O258	I/O259	I/O260
19	GND	I/O261	I/O262	I/O263	I/O264	CT_VCC

95-pin I/O connector according to IEC 1076-4-101

Description of the signals of P0:

(ETH1_MDIx_P), (ETH1_MDIx_N)	...	Ethernet interface 1 (IEEE802.3) (x = 0, 1, 2, 3) (only at VME-PMC-CPU/2-CC, otherwise these pins are not connected)
RXSy, TXSy	...	Serial interfaces 1 and 2 (y = 1, 2), physical layer RS-232 (These signals are bridged to signals of the same name of connector X1940 in the front panel.
I/O201 ... I/O264	...	I/O signals of the PMC slot 2 (J24) according to VITA 35, P4 V0-64

Note:
The signals I/O201...I/O232 can be connected via 1 kΩ-resistor to the FPGA-ports FPGA-XI/O01... FPGA-XI/O32 (only 3.3V-tolerant). Please contact our support team.

FPGA-XI/O33... FPGA-XI/O47	...	I/O-signals directly routed to FPGA, only 3.3V-tolerant (not available at the moment; do not connect)
do not connect	...	Do not connect this pin.
-	...	This pin is not connected on the board.

5.8.4 Standard Assignment of the I/O Connector J14 at PMC Slot 1

Signal		Pin No of J14		Signal	
Name	to P2-Pin			Name	to P2-Pin
I/O101	c1	1	2	I/O102	a1
I/O103	c2	3	4	I/O104	a2
I/O105	c3	5	6	I/O106	a3
I/O107	c4	7	8	I/O108	a4
I/O109	c5	9	10	I/O110	a5
I/O111	c6	11	12	I/O112	a6
I/O113	c7	13	14	I/O114	a7
I/O115	c8	15	16	I/O116	a8
I/O117	c9	17	18	I/O118	a9
I/O119	c10	19	20	I/O120	a10
I/O121	c11	21	22	I/O122	a11
I/O123	c12	23	24	I/O124	a12
I/O125	c13	25	26	I/O126	a13
I/O127	c14	27	28	I/O128	a14
I/O129	c15	29	30	I/O130	a15
I/O131	c16	31	32	I/O132	a16
I/O133	c17	33	34	I/O134	a17
I/O135	c18	35	36	I/O136	a18
I/O137	c19	37	38	I/O138	a19
I/O139	c20	39	40	I/O140	a20
I/O141	c21	41	42	I/O142	a21
I/O143	c22	43	44	I/O144	a22
I/O145	c23	45	46	I/O146	a23
I/O147	c24	47	48	I/O148	a24
I/O149	c25	49	50	I/O150	a25
I/O151	c26	51	52	I/O152	a26
I/O153	c27	53	54	I/O154	a27
I/O155	c28	55	56	I/O156	a28
I/O157	c29	57	58	I/O158	a29
I/O159	c30	59	60	I/O160	a30
I/O161	c31	61	62	I/O162	a31
I/O163	c32	63	64	I/O164	a32

Socket connector 2x32

5.8.5 Standard Assignment of the I/O Connector J24 at PMC Slot 2

Signal		Pin No of J24		Signal	
Name	to P0-Pin			Name	to P0-Pin
I/O201	e4	1	2	I/O202	d4
I/O203	c4	3	4	I/O204	b4
I/O205	a4	5	6	I/O206	e5
I/O207	d5	7	8	I/O208	c5
I/O209	b5	9	10	I/O210	a5
I/O211	e6	11	12	I/O212	d6
I/O213	c6	13	14	I/O214	b6
I/O215	a6	15	16	I/O216	e7
I/O217	d7	17	18	I/O218	c7
I/O219	b7	19	20	I/O220	a7
I/O221	e8	21	22	I/O222	d8
I/O223	c8	23	24	I/O224	b8
I/O225	a8	25	26	I/O226	e12
I/O227	d12	27	28	I/O228	c12
I/O229	b12	29	30	I/O230	a12
I/O231	e13	31	32	I/O232	d13
I/O233	c13	33	34	I/O234	b13
I/O235	a13	35	36	I/O236	e14
I/O237	d14	37	38	I/O238	c14
I/O239	b14	39	40	I/O240	a14
I/O241	e15	41	42	I/O242	d15
I/O243	c15	43	44	I/O244	b15
I/O245	a15	45	46	I/O246	e16
I/O247	d16	47	48	I/O248	c16
I/O249	b16	49	50	I/O250	a16
I/O251	e17	51	52	I/O252	d17
I/O253	c17	53	54	I/O254	b17
I/O255	a17	55	56	I/O256	e18
I/O257	d18	57	58	I/O258	c18
I/O249	b18	59	60	I/O260	a18
I/O261	e19	61	62	I/O262	d19
I/O263	c19	63	64	I/O264	b19

Socket connector 2x32

5.9 Assignment of the I/O-Signals using the‘-32P2’ Option

5.9.1 Assignment VMEbus P2 using ‘-32P2’ Option

Pin	Row z	Row a	Row b	Row c	Row d	Pin
1	-	I/O102+I/O234	+5 V	I/O101+I/O233	-	1
2	GND	I/O104+I/O236	GND	I/O103+I/O235	-	2
3	-	I/O106+I/O238	BRETRY*	I/O105+I/O237	-	3
4	GND	I/O108+I/O240	A24	I/O107+I/O239	-	4
5	-	I/O110+I/O242	A25	I/O109+I/O241	-	5
6	GND	I/O112+I/O244	A26	I/O111+I/O243	-	6
7	-	I/O114+I/O246	A27	I/O113+I/O245	-	7
8	GND	I/O116+I/O248	A28	I/O115+I/O247	-	8
9	-	I/O118+I/O250	A29	I/O117+I/O249	-	9
10	GND	I/O120+I/O252	A30	I/O119+I/O251	-	10
11	-	I/O122+I/O254	A31	I/O121+I/O253	-	11
12	GND	I/O124+I/O256	GND	I/O123+I/O255	-	12
13	-	I/O126+I/O258	+5 V	I/O125+I/O257	-	13
14	GND	I/O128+I/O260	D16	I/O127+I/O259	-	14
15	-	I/O130+I/O262	D17	I/O129+I/O261	-	15
16	GND	I/O132+I/O264	D18	I/O131+I/O263	-	16
17	-	I/O134	D19	I/O133	-	17
18	GND	I/O136	D20	I/O135	-	18
19	-	I/O138	D21	I/O137	-	19
20	GND	I/O140	D22	I/O139	-	20
21	-	I/O142	D23	I/O141	-	21
22	GND	I/O144	GND	I/O143	-	22
23	-	I/O146	D24	I/O145	-	23
24	GND	I/O148	D25	I/O147	-	24
25	-	I/O150	D26	I/O149	-	25
26	GND	I/O152	D27	I/O151	-	26
27	-	I/O154	D28	I/O153	-	27
28	GND	I/O156	D29	I/O155	-	28
29	-	I/O158	D30	I/O157	-	29
30	GND	I/O160	D31	I/O159	-	30
31	-	I/O162	GND	I/O161	GND	31
32	GND	I/O164	+5 V	I/O163	-	32

160-pin VG-connector according to DIN41612
I_{max} per pin : 1.0 A
- ... Signal is not connected on the board

5.9.2 Assignment of a Transfer Module at '-32P2' Option

The following table shows the assignment of a 64-pin transfer module when connected to the P2 connector. The 64 contacts of the module are connected to the signals of the rows a and c of the connector P2.

Assignment of a 64-pin Transfer Module					
Pin	Assignment of the I/O Connector P2				Pin
	Row a	Signal		Row c	
2	1	I/O102+I/O234	I/O101+I/O233	1	1
4	2	I/O104+I/O236	I/O103+I/O235	2	3
6	3	I/O106+I/O238	I/O105+I/O237	3	5
8	4	I/O108+I/O240	I/O107+I/O239	4	7
10	5	I/O110+I/O242	I/O109+I/O241	5	9
12	6	I/O112+I/O244	I/O111+I/O243	6	11
14	7	I/O114+I/O246	I/O113+I/O245	7	13
16	8	I/O116+I/O248	I/O115+I/O247	8	15
18	9	I/O118+I/O250	I/O117+I/O249	9	17
20	10	I/O120+I/O252	I/O119+I/O251	10	19
22	11	I/O122+I/O254	I/O121+I/O253	11	21
24	12	I/O124+I/O256	I/O123+I/O255	12	23
26	13	I/O126+I/O258	I/O125+I/O257	13	25
28	14	I/O128+I/O260	I/O127+I/O259	14	27
30	15	I/O130+I/O262	I/O129+I/O261	15	29
32	16	I/O132+I/O264	I/O131+I/O263	16	31
34	17	I/O134	I/O133	17	33
36	18	I/O136	I/O135	18	35
38	19	I/O138	I/O137	19	37
40	20	I/O140	I/O139	20	39
42	21	I/O142	I/O141	21	41
44	22	I/O144	I/O143	22	43
46	23	I/O146	I/O145	23	45
48	24	I/O148	I/O147	24	47
50	25	I/O150	I/O149	25	49
52	26	I/O152	I/O151	26	51
54	27	I/O154	I/O153	27	53
56	28	I/O156	I/O155	28	55
58	29	I/O158	I/O157	29	57
60	30	I/O160	I/O159	30	59
62	31	I/O162	I/O161	31	61
64	32	I/O164	I/O163	32	63

5.9.3 Assignment VMEbus P0 at '-32P2' Option

Pin	Row f	Row e	Row d	Row c	Row b	Row a
1	GND	-	-	GND	-	-
2	GND	-	-	GND	-	-
3	GND	RXS2	TXS2	RXS1	TXS1	GND
4	GND	I/O201	I/O202	I/O203	I/O204	I/O205
5	GND	I/O206	I/O207	I/O208	I/O209	I/O210
6	GND	I/O211	I/O212	I/O213	I/O214	I/O215
7	GND	I/O216	I/O217	I/O218	I/O219	I/O220
8	GND	I/O221	I/O222	I/O223	I/O224	I/O225
9	GND	FPGA-XI/O41	FPGA-XI/O42	FPGA-XI/O43	FPGA-XI/O46	FPGA-XI/O47
10	GND	FPGA-XI/O38	FPGA-XI/O39	FPGA-XI/O40	FPGA-XI/O44	FPGA-XI/O45
11	GND	FPGA-XI/O35	FPGA-XI/O36	FPGA-XI/O37	FPGA-XI/O34	FPGA-XI/O33
12	GND	I/O226	I/O227	I/O228	I/O229	I/O230
13	GND	I/O231	I/O232	I/O101+I/O233	I/O102+I/O234	I/O103+I/O235
14	GND	I/O104+I/O236	I/O105+I/O237	I/O106+I/O238	I/O107+I/O239	I/O108+I/O240
15	GND	I/O109+I/O241	I/O110+I/O242	I/O111+I/O243	I/O112+I/O244	I/O113+I/O245
16	GND	I/O114+I/O246	I/O115+I/O247	I/O116+I/O248	I/O117+I/O249	I/O118+I/O250
17	GND	I/O119+I/O251	I/O120+I/O252	I/O121+I/O253	I/O122+I/O254	I/O123+I/O255
18	GND	I/O124+I/O256	I/O125+I/O257	I/O126+I/O258	I/O127+I/O259	I/O128+I/O260
19	GND	I/O129+I/O261	I/O130+I/O262	I/O131+I/O263	I/O132+I/O264	do not connect

95-pin I/O connector according to IEC 1076-4-101

Description of the signals of P0:

RXSy, TXSy...	Serial interfaces 1 and 2 (y = 1, 2), physical layer RS-232 (These signals are bridged to the signals of the same name of connector X1940 in the front panel.
I/O201 ... I/O232...	I/O-signals of PMC slot 2 (J24)
I/O101+I/O233 ... I/O132+I/O264...	Bridged I/O-signals of the PMC slots 1 (J14) and 2 (J24)
FPGA-XI/O33 FPGA-XI/O47...	I/O-signals directly to FPGA, only 3.3V-tolerant (not available at the moment; do not connect)
do not connect...	Do not connect this pin.
-...	This pins is not connected on the board.

5.9.4 Assignment of the PMC Connector J14 at '-32P2' Option

Signal										Signal					
Name			P2-Pin		P0-Pin	J24-Pin	**J14-Pin**		J24-Pin	P2-Pin		P0-Pin	Name		
I/O101	+	I/O233	c1	+	c13	33	**1**	**2**	34	a1	+	b13	I/O102	+	I/O234
I/O103	+	I/O235	c2	+	a13	35	**3**	**4**	36	a2	+	e14	I/O104	+	I/O236
I/O105	+	I/O237	c3	+	d14	37	**5**	**6**	38	a3	+	c14	I/O106	+	I/O238
I/O107	+	I/O239	c4	+	b14	39	**7**	**8**	40	a4	+	a14	I/O108	+	I/O240
I/O109	+	I/O241	c5	+	e15	41	**9**	**10**	42	a5	+	d15	I/O110	+	I/O242
I/O111	+	I/O243	c6	+	c15	43	**11**	**12**	44	a6	+	b15	I/O112	+	I/O244
I/O113	+	I/O245	c7	+	a15	45	**13**	**14**	46	a7	+	e16	I/O114	+	I/O246
I/O115	+	I/O247	c8	+	d16	47	**15**	**16**	48	a8	+	c16	I/O116	+	I/O248
I/O117	+	I/O249	c9	+	b16	49	**17**	**18**	50	a9	+	a16	I/O118	+	I/O250
I/O119	+	I/O251	c10	+	e17	51	**19**	**20**	52	a10	+	d17	I/O120	+	I/O252
I/O121	+	I/O253	c11	+	c17	53	**21**	**22**	54	a11	+	b17	I/O122	+	I/O254
I/O123	+	I/O255	c12	+	a17	55	**23**	**24**	56	a12	+	e18	I/O124	+	I/O256
I/O125	+	I/O257	c13	+	d18	57	**25**	**26**	58	a13	+	c18	I/O126	+	I/O258
I/O127	+	I/O249	c14	+	b18	59	**27**	**28**	60	a14	+	a18	I/O128	+	I/O260
I/O129	+	I/O261	c15	+	e19	61	**29**	**30**	62	a15	+	d19	I/O130	+	I/O262
I/O131	+	I/O263	c16	+	c19	63	**31**	**32**	64	a16	+	b19	I/O132	+	I/O264
I/O133			c17				**33**	**34**		a17			I/O134		
I/O135			c18				**35**	**36**		a18			I/O136		
I/O137			c19				**37**	**38**		a19			I/O138		
I/O139			c20				**39**	**40**		a20			I/O140		
I/O141			c21				**41**	**42**		a21			I/O142		
I/O143			c22				**43**	**44**		a22			I/O144		
I/O145			c23				**45**	**46**		a23			I/O146		
I/O147			c24				**47**	**48**		a24			I/O148		
I/O149			c25				**49**	**50**		a25			I/O150		
I/O151			c26				**51**	**52**		a26			I/O152		
I/O153			c27				**53**	**54**		a27			I/O154		
I/O155			c28				**55**	**56**		a28			I/O156		
I/O157			c29				**57**	**58**		a29			I/O158		
I/O159			c30				**59**	**60**		a30			I/O160		
I/O161			c31				**61**	**62**		a31			I/O162		
I/O163			c32				**63**	**64**		a32			I/O164		

Socket connector 2x32

Reading the Table - Examples:
Pin 9 of the PMC connector J14 is connected with pin 41 of the PMC connector J24. Furthermore pin 9 is connected to the pins c5 and z27 of the VMEbus connector P2. In the schematic diagram the signal names I/O109 and I/O241 are used for this net.

5.9.5 Assignment of the PMC Connector J24 at '-32P2' Option

Signal														Signal
Name			P2-Pin		P0-Pin	J14-Pin	J24-Pin		J14-Pin	P2-Pin		P0-Pin		Name
I/O201					e4		1	2				d4		I/O202
I/O203					c4		3	4				b4		I/O204
I/O205					a4		5	6				e5		I/O206
I/O207					d5		7	8				c5		I/O208
I/O209					b5		9	10				a5		I/O210
I/O211					e6		11	12				d6		I/O212
I/O213					c6		13	14				b6		I/O214
I/O215					a6		15	16				e7		I/O216
I/O217					d7		17	18				c7		I/O218
I/O219					b7		19	20				a7		I/O220
I/O221					e8		21	22				d8		I/O222
I/O223					c8		23	24				b8		I/O224
I/O225					a8		25	26				e12		I/O226
I/O227					d12		27	28				c12		I/O228
I/O229					b12		29	30				a12		I/O230
I/O231					e13		31	32				d13		I/O232
I/O233	+	I/O101	c1	+	c13	1	33	34	2	a1	+	b13	+	I/O234 + I/O102
I/O235	+	I/O103	c2	+	a13	3	35	36	4	a2	+	e14	+	I/O236 + I/O104
I/O237	+	I/O105	c3	+	d14	5	37	38	6	a3	+	c14	+	I/O238 + I/O106
I/O239	+	I/O107	c4	+	b14	7	39	40	8	a4	+	a14	+	I/O240 + I/O108
I/O241	+	I/O109	c5	+	e15	9	41	42	10	a5	+	d15	+	I/O242 + I/O110
I/O243	+	I/O111	c6	+	c15	11	43	44	12	a6	+	b15	+	I/O244 + I/O112
I/O245	+	I/O113	c7	+	a15	13	45	46	14	a7	+	e16	+	I/O246 + I/O114
I/O247	+	I/O115	c8	+	d16	15	47	48	16	a8	+	c16	+	I/O248 + I/O116
I/O249	+	I/O117	c9	+	b16	17	49	50	18	a9	+	a16	+	I/O250 + I/O118
I/O251	+	I/O119	c10	+	e17	19	51	52	20	a10	+	d17	+	I/O252 + I/O120
I/O253	+	I/O121	c11	+	c17	21	53	54	22	a11	+	b17	+	I/O254 + I/O122
I/O255	+	I/O123	c12	+	a17	23	55	56	24	a12	+	e18	+	I/O256 + I/O124
I/O257	+	I/O125	c13	+	d18	25	57	58	26	a13	+	c18	+	I/O258 + I/O126
I/O249	+	I/O127	c14	+	b18	27	59	60	28	a14	+	a18	+	I/O260 + I/O128
I/O261	+	I/O129	c15	+	e19	29	61	62	30	a15	+	d19	+	I/O262 + I/O130
I/O263	+	I/O131	c16	+	c19	31	63	64	32	a16	+	b19	+	I/O264 + I/O132

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5.10 Special Assembly: J24-I/O-Signals to d+z of P2 (acc. VITA 35, P4 V2-46dz)

5.10.1 Assignment of P2 at Special Assembly with RC800, RC801, ...RC811

In this special assembly the I/O signals of the PMC slot 2 (J24) are not only connected to P0 but in parallel to this also to the rows d+z of P2.
For this assembly there is currently no ordering option specified. Please contact our sales team (sales@esd.eu) if you are interested in this special option.

Pin	Row z	Row a	Row b	Row c	Row d	Pin
1	I/O202	I/O102	+5 V	I/O101	I/O201	1
2	GND	I/O104	GND	I/O103	I/O203	2
3	I/O205	I/O106	BRETRY*	I/O105	I/O204	3
4	GND	I/O108	A24	I/O107	I/O206	4
5	I/O208	I/O110	A25	I/O109	I/O207	5
6	GND	I/O112	A26	I/O111	I/O209	6
7	I/O211	I/O114	A27	I/O113	I/O210	7
8	GND	I/O116	A28	I/O115	I/O212	8
9	I/O214	I/O118	A29	I/O117	I/O213	9
10	GND	I/O120	A30	I/O119	I/O215	10
11	I/O217	I/O122	A31	I/O121	I/O216	11
12	GND	I/O124	GND	I/O123	I/O218	12
13	I/O220	I/O126	+5 V	I/O125	I/O219	13
14	GND	I/O128	D16	I/O127	I/O221	14
15	I/O223	I/O130	D17	I/O129	I/O222	15
16	GND	I/O132	D18	I/O131	I/O224	16
17	I/O226	I/O134	D19	I/O133	I/O225	17
18	GND	I/O136	D20	I/O135	I/O227	18
19	I/O229	I/O138	D21	I/O137	I/O228	19
20	GND	I/O140	D22	I/O139	I/O230	20
21	I/O232	I/O142	D23	I/O141	I/O231	21
22	GND	I/O144	GND	I/O143	I/O233	22
23	I/O235	I/O146	D24	I/O145	I/O234	23
24	GND	I/O148	D25	I/O147	I/O236	24
25	I/O238	I/O150	D26	I/O149	I/O237	25
26	GND	I/O152	D27	I/O151	I/O239	26
27	I/O241	I/O154	D28	I/O153	I/O240	27
28	GND	I/O156	D29	I/O155	I/O242	28
29	I/O244	I/O158	D30	I/O157	I/O243	29
30	GND	I/O160	D31	I/O159	I/O245	30
31	I/O246	I/O162	GND	I/O161	GND	31
32	GND	I/O164	+5 V	I/O163	-	32

160-pin VG-connector according to DIN41612
I_{max} per pin : 1.0 A
- ... Signal is not connected on the board

5.10.2 Assignment I/O Connector J24 at Assembly with RC800, RC801, ...RC811

Signal				Signal	
Name	to P2-Pin	J24-Pin		Name	to P2-Pin
I/O201	d1	1	2	I/O202	z1
I/O203	d2	3	4	I/O204	d3
I/O205	z3	5	6	I/O206	d4
I/O207	d5	7	8	I/O208	z5
I/O209	d6	9	10	I/O210	d7
I/O211	z7	11	12	I/O212	d8
I/O213	d9	13	14	I/O214	z9
I/O215	d10	15	16	I/O216	d11
I/O217	z11	17	18	I/O218	d12
I/O219	d13	19	20	I/O220	z13
I/O221	d14	21	22	I/O222	d15
I/O223	z15	23	24	I/O224	d16
I/O225	d17	25	26	I/O226	z17
I/O227	d18	27	28	I/O228	d19
I/O229	z19	29	30	I/O230	d20
I/O231	d21	31	32	I/O232	z21
I/O233	d22	33	34	I/O234	d23
I/O235	z23	35	36	I/O236	d24
I/O237	d25	37	38	I/O238	z25
I/O239	d26	39	40	I/O240	d27
I/O241	z27	41	42	I/O242	d28
I/O243	d29	43	44	I/O244	z29
I/O245	d30	45	46	I/O246	z31
I/O247	-	47	48	I/O248	-
I/O249	-	49	50	I/O250	-
I/O251	-	51	52	I/O252	-
I/O253	-	53	54	I/O254	-
I/O255	-	55	56	I/O256	-
I/O257	-	57	58	I/O258	-
I/O249	-	59	60	I/O260	-
I/O261	-	61	62	I/O262	-
I/O263	-	63	64	I/O264	-

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5.11 XMC Socket J15

Pin	Row					
	a	b	c	d	e	f
1	PER_0_P	PER_0_N	3,3V	PER_1_P	PER_1_N	VPWR
2	GND	GND	PCI-TRST#	GND	GND	PORST#
3	PER_2_P	PER_2_N	3,3V	PER_3_P	PWER_3_N	VPWR
4	GND	GND	PCI-TCK	GND	GND	XMC_RSTO#
5	-	-	3,3V	-	-	VPWR
6	GND	GND	PCI-TMS	GND	GND	+12V
7	-	-	3,3V	-	-	VPWR
8	GND	GND	PCI-TD2	GND	GND	-12V
9	-	-	-	-	-	VPWR
10	GND	GND	PCI-TDO	GND	GND	GND
11	PET_0_P	PET_0_N	XMC_BIST#	PET_1_P	PET_1_N	VPWR
12	GND	GND	GND	GND	GND	XMC_PRSNT#
13	PET_2_P	PET_2_N	3,3VAUX	PET_3_P	PET_3_N	VPWR
14	GND	GND	3,3V	GND	GND	IIC2_SDA
15	-	-	-	-	-	VPWR
16	GND	GND	GND	GND	GND	IIC2_SCL
17	-	-	-	-	-	-
18	GND	GND	-	GND	GND	-
19	REFCLK_1_P	REF_CLK_1_N	-	-	-	-

Signal Description of J15:

PER_x_P, PER_x_N...	Differential PCI EXPRESS receiver signals (x = 0, 1, 2, 3) of the four lanes.
PET_x_P, PET_x_N...	Differential PCI EXPRESS transmitter signals (x = 0, 1, 2, 3) of the four lanes.
PCI-TRST#...	
PORST#...	Card Reset
PCI-TCK, PCI-TD2, PCI-TMS...	PCI-JTAG-Interface
XMC_RSTO# ...	This signal is triggered by the XMC card.
XMC_BIST#...	This pin is not connected on the board.
XMC_PRSNT#...	PMC module detection signal
IIC2_SDA, IIC2_SCL...	I²C data- and clock signal (IPMI support)
REFCLK_1_P, REFCLK_1_N...	100 MHz PCI-EXPRESS Reference Clock
GND...	Reference potential
VPWR...	Power supply voltage +5V (selectable via solder bridges, VPWR can be alternatively connected to the 12V supply voltage of the VMEbus; please contact our sales team for this)
3.3V...	Power supply voltage +3.3V
3.3VAUX...	3.3V AUX generated of +5V STBY supplied by VMEbus
+12V/-12V...	Power supply voltage +12V and -12V
-...	These pins are not connected on the board.

6. References

[1] Tsi148™PCI/X-to-VME Bus Bridge User Manual,
Tundra Semiconductor Corporation,
referenced document version: 80A3020_MA001_10, April 2008
document source: http://www.idt.com/

[2] MPC8349E PowerQUICC™ II Pro, Integrated Host Processor, Family Reference Manual,
Freescale Semiconductor,
Rev. 1, 8/2005,
document source: http://www.freescale.com

7. Order Information

Type	Properties	Order No.
VME-PMC-CPU/2	VMEbus-CPU, 2 PMC modules, PPMC, XMC, 2x Ethernet, 2x USB, RS-232 standard temperature range (0...+50 °C)	V.1917.01
VME-PMC-CPU/2-T-40/75	As V.1917.01, but for extended temperature range (-40...+75 °C)	V.1917.02
VME-PMC-CPU/2-CC	VMEbus-CPU, 2 PMC modules, PPMC, XMC RS-232, Conduction Cooled Version, extended temperature range (-40...+75 °C)	V.1917.03
VME-PMC-CPU/2-32P2	as V.1917.01, but assignment of the rows a and c of P2 connector according to IEEE Std 1386-2001/Table 8	V.1917.11
VME-PMC-CPU/2-46dz	6HE VMEbus CPU, 533 MHz MPC 8349, 2 Slots: 2x PMC o. 1x PMC,1x XMC, 2x Gbit Eth, 2x USB 2.0, 2x RS-232, FPGA XC3S1600E, RTC buffered, incl. Underfilling, Coating	V.1917.12
VME-PMC-CPU/2-T-40/75+32P2	as V.1917.02, but assignment of the rows a and c of P2 connector according to IEEE Std 1386-2001/Table 8	V.1917.13
VME-PMC-CPU/2-CC CC + 32P2	VME-PMC-CPU/2-CC CC + 32P2	V.1917.14
Software Drivers		
VME-PMC-CPU/2 Linux BSP	VME-PMC-CPU/2 Linux BSP	V.1917.57
VME-PMC-CPU/2 VxWorks BSP	VME-PMC-CPU/2 VxWorks LIB Library for VxWorks to support access to PCI-Devices as C-Source	V.1917.58

For detailed information about the driver availability for your operating system, please contact our sales team.

Table 19: Order information

PDF Manuals
Manuals are available in English and usually in German as well. Available manuals are listed in the following table.
Please download the manuals as PDF documents from our esd website www.esd.eu for free.

Manuals		Order No.
VME-PMC-CPU/2-MD	Hardware manual in German	V.1917.20
VME-PMC-CPU/2-ME	Hardware manual in English	V.1917.21

Table 20: Available manuals

Printed Manuals
If you need a printout of the manual additionally, please contact our sales team: sales@esd.eu for a quotation. Printed manuals may be ordered for a fee.