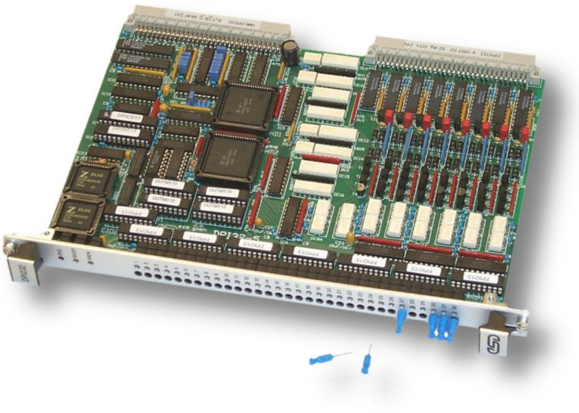
VME-DPIO32/63140

32 digital Inputs or Outputs



Hardware Manual

to Product V.1607.04

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NOTE

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⚠	This manual contains important information and instructions on safe and efficient handling of the VME-DPIO32/63140. Carefully read this manual before commencing any work and follow the instructions. The manual is a product component, please retain it for future use.

Trademark Notices

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Document History

The changes in the document listed below affect changes in the hardware as well as changes in the description of the facts, only.

Rev.	Chapter	Changes versus previous version	Date
2.2	-	Safety Instructions and Information and Classification of Warning messages inserted, Manual restructured	2016-03-11
	1.	Block circuit diagram new, text according to data sheet	
	2.	Chapter “Technical Data” revised	
	3.	Chapter “Hardware Configuration” revised	
	4.	Chapter “Interrupt Processing”, description of HD63140 and figure changed	
	5.	Chapter “Digital Inputs and Outputs” description of HD63140	
	6.	New Chapter “Hardware Installation”	
	7.	Chapter “Connector Pin Assigments”	
	8.	Chapter “Order Information” moved and revised	

Technical details are subject to change without further notice.

Classification of Warning Messages and Safety Instructions

This manual contains noticeable descriptions, warning messages and safety instructions, which you must follow to avoid personal injuries or death and property damage.

This is the safety alert symbol.
It is used to alert you to potential personal injury hazards. Obey all safety messages and instructions that follow this symbol to avoid possible injury or death.

DANGER, WARNING, CAUTION

Depending on the hazard level the signal words DANGER, WARNING or CAUTION are used to highlight safety instructions and warning messages. These messages may also include a warning relating to property damage.

DANGER
Danger statements indicate a hazardous situation which, if not avoided, will result in death or serious injury.

WARNING
Warning statements indicate a hazardous situation that, if not avoided, could result in death or serious injury.

CAUTION
Caution statements indicate a hazardous situation that, if not avoided, could result in minor or moderate injury.

NOTICE

Notice statements are used to notify people on hazards that could result in things other than personal injury, like property damage.

NOTICE
This NOTICE statement indicates that the device contains components sensitive to electrostatic discharge.

NOTICE
This NOTICE statement contains the general mandatory sign and gives information that must be heeded and complied with for a safe use.

INFORMATION

INFORMATION
Notes to point out something important or useful.

Safety Instructions

- When working with the VME-DPIO32/63140 follow the instructions below and read the manual carefully to protect yourself from injury and the VME-DPIO32/63140 from damage.
- The device is a built-in component. It is essential to ensure that the device is mounted in a way that cannot lead to endangering or injury of persons or damage to objects.
- Do not use damaged or defective cables to connect the VME-DPIO32/63140.
- In case of damages to the device, which might affect safety, appropriate and immediate measures must be taken, that exclude an endangerment of persons and domestic animals and property.
- Current circuits which are connected to the device have to be sufficiently protected against hazardous voltage (SELV according to EN 60950-1).
- The VME-DPIO32/63140 may only be driven by power supply current circuits, that are contact protected.
  A power supply, that provides a safety extra-low voltage (SELV) according to EN 60950-1, complies with this conditions.

- The device has to be securely installed in the control cabinet before commissioning.
- Protect the VME-DPIO32/63140 from dust, moisture and steam.
- Protect the VME-DPIO32/63140 from shocks and vibrations.
- The VME-DPIO32/63140 may become warm during normal use. Always allow adequate ventilation around the VME-DPIO32/63140 and use care when handling.
- Do not operate the VME-DPIO32/63140 adjacent to heat sources and do not expose it to unnecessary thermal radiation. Ensure an ambient temperature as specified in the technical data.

DANGER
Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the VME-DPIO32/63140 is to be integrated.
→ Disconnect all hazardous voltages (mains voltage) before opening the system.
→ Ensure the absence of voltage before starting any electrical work

NOTICE
Electrostatic discharges may cause damage to electronic components.
To avoid this, perform the steps described on page 30 *before* you touch the VME-DPIO32/63140, in order to discharge the static electricity from your body.

Qualified Personal

This documentation is directed exclusively towards personal qualified in control and automation engineering. The installation and commissioning of the product may only be carried out by qualified personal, which is authorized to put devices, systems and electric circuits into operation according to the applicable national standards of safety engineering.

Conformity

The VME-DPIO32/63140 is a sub-assembly intended for incorporation into an apparatus by a manufacturer and NOT by the end user. The manufacturer of the final system must decide, whether additional EMC or EMI protection requirements are necessary.

Intended Use

The intended use of the VME-DPIO32/63140 is the operation as VME board with digital I/Os.
The guarantee given by esd does not cover damages which result from improper use, usage not in accordance with regulations or disregard of safety instructions and warnings.

- The VME-DPIO32/63140 is intended for installation in VMEbus systems only.
- The operation of the VME-DPIO32/63140 in hazardous areas, or areas exposed to potentially explosive materials is not permitted.
- The operation of the VME-DPIO32/63140 for medical purposes is prohibited.

Service Note

The VME-DPIO32/63140 does not contain any parts that require maintenance by the user. The VME-DPIO32/63140 does not require any manual configuration of the hardware. Unauthorized intervention in the device voids warranty claims.

Disposal

Devices which have become defective in the long run have to be disposed in an appropriate way or have to be returned to the manufacturer for proper disposal. Please, make a contribution to environmental protection.

Table of contents

1. Overview

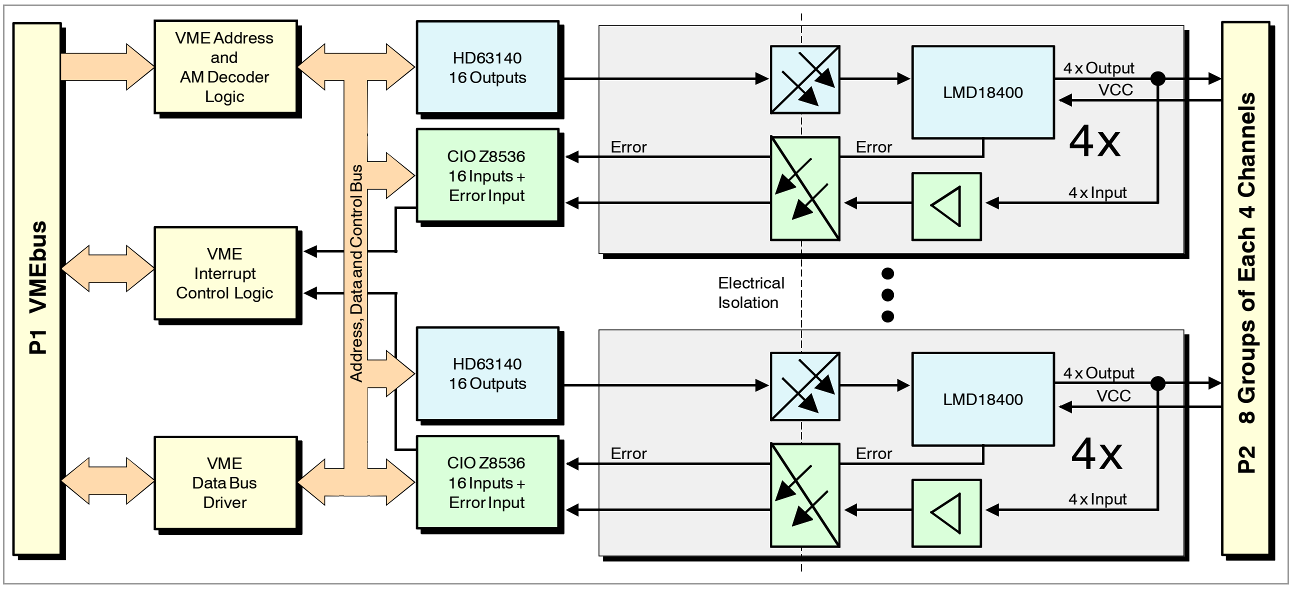

P1 VMEbus
VME Address and AM Decoder Logic
VME Interrupt Control Logic
VME Data Bus Driver
Address, Data and Control Bus
HD63140 16 Outputs
CIO Z8536 16 Inputs + Error Input
Error
Error
LMD18400
4 x Output
VCC
4x
4 x Input
Electrical Isolation
P2 8 Groups of Each 4 Channels

Figure 1: Block circuit diagram of VME-DPIO32/63140

The VME-DPIO32/63140 offers a digital process interface containing 32 optoisolated digital process I/O channels. It includes all necessary components on a VMEbus 6U board and needs one slot.

The 32 digital I/O channels are programmable in 8 groups of 4 channels as inputs or outputs. The 8 groups are electrically isolated from each other.
The input channels accept an input voltage range of 5 VDC to 30 VDC. Each input channel can generate an interrupt on the VMEbus and that is programmable to rising or to falling edge. The inputs are overvoltage protected between -3 VDC and +35 VDC. The digital output channels accept an operating voltage range of 6 VDC to 28 VDC with a rated current of 0.3 A.

The outputs are driven by Quad High Side Drivers LMD18400. The protection circuit of the driver is activated by short-circuit, over temperature and overvoltage. An error signal will be generated by the drivers on the following conditions: no load, short circuit to GND, to VCC, overvoltage or over temperature of the driver module.

In addition to the bit programmable operating mode of the outputs, it is possible to use the single output channels via the pulse processor components HD63140 for pulse-width modulation (PWM). A total of 2 x 24 programmable 16 bit registers for switching period and resolution are available. The minimum pulse width amounts to 10 :s. The outputs can be synchronized.

Up to 4 digital inputs may be used as counter inputs at the CIO8536. The maximum counter frequency for the inputs is 3 MHz.

The actual I/O status and error status of each I/O channel is displayed by a two coloured LED on the front panel of the VME-DPIO32/63140.

Additionally, there are test sockets for each channel located on the front panel for stimulation of the input channels or for disable of the output driver error signal.

The 64-pin adapter blocks VME-P2-ADAPT1 or VME-P2-ADAPT1 are connected via ribbon cable to the P2 connector of the VME-DPIO32/63140. They offer wiring with screw or clamp terminals for all P2 I/O signals.
To feed power supply for the 8 output groups separately (4 outputs are combined to one group) the power adapter VMEDPIO32-P2VCC is used.

If a separate wiring of the output groups is not necessary the adapter VME-DPIO32-P2VCC-3X feeds power to 3 VME-DPIO32/63140 installed in 3 VMEbus slots side-by-side is an economic solution.

2. Technical Data

2.1 General Technical Data

Digital power supply voltage	VMEbus P1: 5V ± 5% (typical values at 20 °C):	
	all outputs OFF:	1.7 A
	all outputs ON:	2.3 A
	16 outputs ON, 16 OFF:	1.7 A
	all outputs OFF, all inputs ON:	2.3 A
Electrical isolation of inputs and outputs	Pollution degree:	Pollution degree: 2 (acc. to DIN EN 61131-2)
	Over voltage category:	II (acc. to DIN EN 61131-2)
	Electrical isolation:	functional isolation between I/O circuits and VMEbus, dimensioning of air and creepage distances: max. isolation working voltage Ue = 600 V AC/DC (acc. to. DIN EN 61131-2, pollution degree 2, over voltage category II) max. isolation voltage of optocouplers U_{rms} = 2500 V_{rms} for 1 minute
Connector types	P1-DIN 41612-C96 P2-DIN 41612-C64	
Temperature range	0...70 °C ambient temperature	
Humidity	max. 90%, non-condensing	
Board size	160 mm x 233 mm	
VME dimensions	6 U height / 1 slot width	
Weight	470 g	

Table 1: General data of the module

2.2 VME specification

VME interface	IEEE 1014 / D
Data transfer mode	SADO24 - slave with A24/D16 access SD16 - slave with A16/D16 access
Address modifier (AM)	full evaluation of AM0 to AM5, additionally 'AM2 don't care' circuit possible
Basic address	selectable by jumpers over the whole address range of 16 Mbytes, the board covers 4 kbytes
Interrupts	I1 to I7 interrupter, level programmable via HD63140

Table 2: VME interface

2.3 Digital Outputs

Quantity	32 (less inputs) P-switching: Out = 24 V --> ’1’ Out = 0 V --> ’0’
Supply voltage	U_{vccmin} = 6 V (DC) U_{vccmax} = 28 V (DC) $U_{vccrated}$ = 24 V (DC)
Load capacity (at 50°C)	rated current/channel (24 V): I_r = 0.3 A, max. current/channel: limited by overtemperature protection (see data sheet of LMD18400) max. current/board: 16 A signal level of outputs at rated current: ≥ U_{vcc}-2 V
Protective circuits	short-circuit protection and overtemperature protection: electronically with switch-off of output group, overvoltage protection (triggering from U_{vcc} > 32 V..35 V)
Switching performance (at 20°)	values for $U_{vccrated}$ and I_r: min. pulse time T ≥ 10 µs, min. clock period T_{ON} ≥ 10 µs, T_{OFF} ≥ 10 µs (With this switching times the signal edges are bad. Additionally the times may become longer due to circuit tolerance and ambient temperature.)
Electrical isolation from VMEbus potential	see description of electrical isolation in chapter “General Technical Data”, page 10

Table 3: Data of the digital outputs

2.4 Digital Inputs

Quantity	32 (less outputs)
Evaluation	all inputs have interrupt capability max. 16 inputs at P2 configurable as counter inputs, all 16 inputs connected to HD63140 and additionally 4 inputs in parallel to CIO Z8536 (higher resolution)
Input voltage	permissible input voltage range: $-3\ V \le U_{in} \le 30\ V$ **Attention:** If output driver LMD18400 is supplied by U_{vccout}, U_{in} may not exceed $\mathbf{U_{in} \le U_{vccout} - 2V}$! (because of parallel connection to outputs) threshold input = ’0’: $U_{out} \le 2.0V$ threshold input = ’1’: $U_{in} \ge 3.0V$
Input current	Since the inputs and outputs are connected in parallel on the board, the input current depends on the fact, whether the supply voltage is connected to the output driver LMD18400: input current/channel at U*vcc* = 24 V (typical values at 20 °C): input = ’1’: (5 V) I_{in} = 7.7 mA (12 V) I_{in} = 9.9 mA (22 V) I_{in} = 10.0 mA input current/channel at U*vcc* not supplied (typical values at 20 °C): input = ’1’: (5 V) I_{in} = 8.0 mA (12 V) I_{in} = 14.0 mA (24 V) I_{in} = 30.0 mA (30 V) I_{in} = 40.0 mA
Input frequency	input circuit (max.): 1 MHz (1:1) counter frequency of controller HD63140 (depends on the complexity of the functions): just one function: t_{high} > 0.5 µs, t_{low} > 0.5 µs f_{max} < 1 MHz (duty cycle 1:1) 16 functions: t_{high} > 5.0 µs, t_{low} > 5.0 µs f_{max} < 100 kHz (duty cycle 1:1) counter frequency of controller CIO 8536 max. 3 MHz
protective circuit	overvoltage protection by Transsil diode voltage-proof up to... statically: U_{max} = 36 V dynamically: U_{max} = 95 V (duty cycle 1/100, ton = 10 µs) U_{max} = 225 V (duty cycle 1/1000, ton = 10 µs)
Electrical isolation from VMEbus potential	see description of electrical isolation in chapter “General Technical Data”, page 10

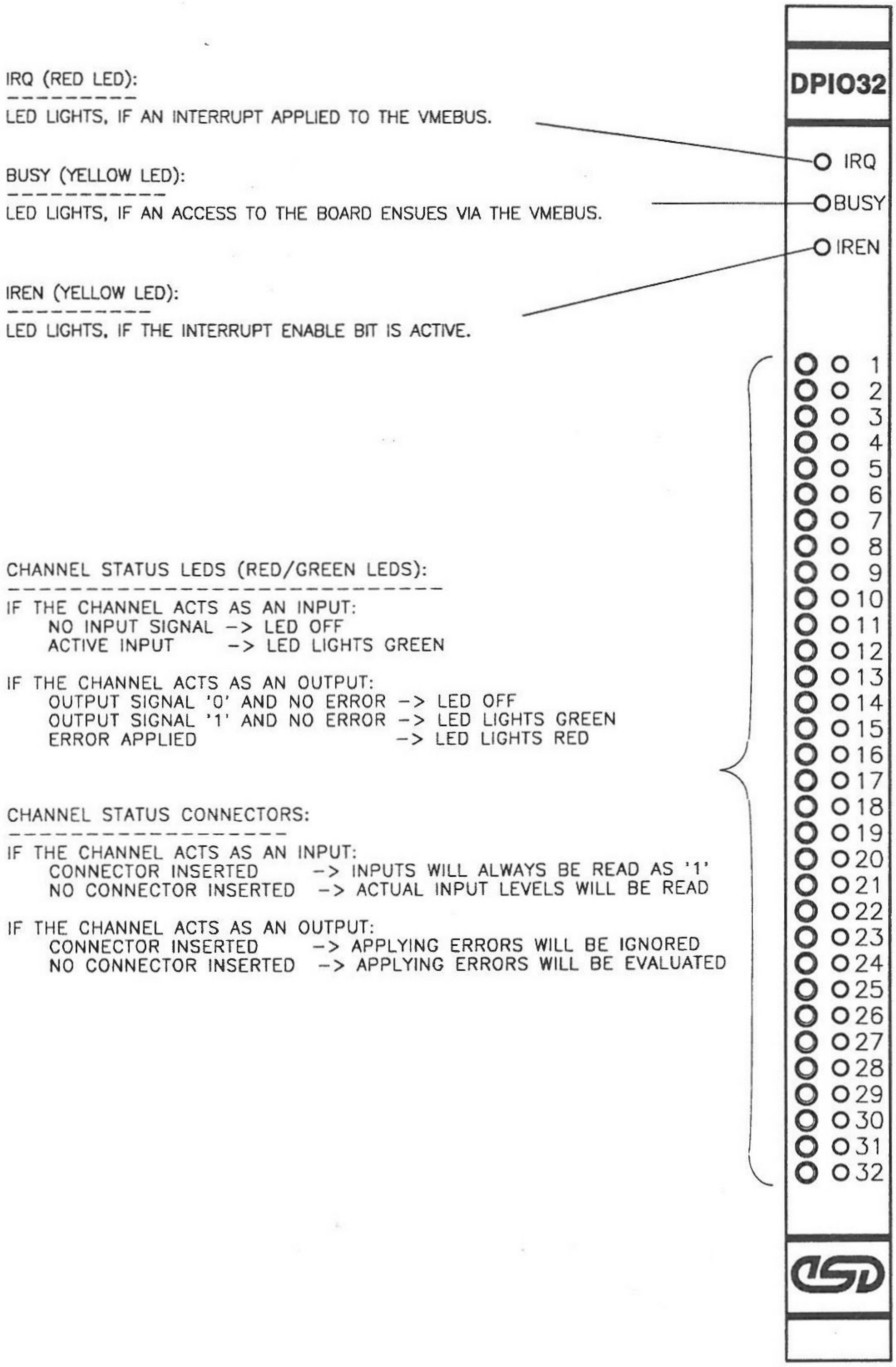
Table 4: Data of the digital inputs

2.5 Software Support

Driver packages for VME-DPIO32/63140 are available e.g. for operating systems VxWorks and OS9.

3. Hardware Configuration

3.1 Front Panel View with LEDs



IRQ (RED LED):

LED LIGHTS, IF AN INTERRUPT APPLIED TO THE VMEBUS.

BUSY (YELLOW LED):

LED LIGHTS, IF AN ACCESS TO THE BOARD ENSUES VIA THE VMEBUS.

IREN (YELLOW LED):

LED LIGHTS, IF THE INTERRUPT ENABLE BIT IS ACTIVE.

CHANNEL STATUS LEDS (RED/GREEN LEDS):

IF THE CHANNEL ACTS AS AN INPUT:
NO INPUT SIGNAL -> LED OFF
ACTIVE INPUT -> LED LIGHTS GREEN

IF THE CHANNEL ACTS AS AN OUTPUT:
OUTPUT SIGNAL '0' AND NO ERROR -> LED OFF
OUTPUT SIGNAL '1' AND NO ERROR -> LED LIGHTS GREEN
ERROR APPLIED -> LED LIGHTS RED

CHANNEL STATUS CONNECTORS:

IF THE CHANNEL ACTS AS AN INPUT:
CONNECTOR INSERTED -> INPUTS WILL ALWAYS BE READ AS '1'
NO CONNECTOR INSERTED -> ACTUAL INPUT LEVELS WILL BE READ

IF THE CHANNEL ACTS AS AN OUTPUT:
CONNECTOR INSERTED -> APPLYING ERRORS WILL BE IGNORED
NO CONNECTOR INSERTED -> APPLYING ERRORS WILL BE EVALUATED

Figure 2: Front panel view

NOTICE
Read chapter “Hardware Installation” on page 30, before you start with the installation of the hardware!

3.2 Address Covering of VME-DPIO32/63140

Address range	D15-D8	D7-D0
nn ss FE nn ss F8	CIO2 (Z8536)	CIO1 (Z8536)
nn ss F6 nn ss F0	RAM of HD2 (HD63140)	RAM of HD1 (HD63140)
nn ss DE nn ss 00	HD2 (HD63140)	HD1 (HD63140)

Table 5: Address Covering of VME-DPIO32/63140

nn ss .... basic address of DPIO32 for ’standard address accesses’
via VMEbus (A08 - A23 = CARD-ADDRESS)
ss .... basic address of DPIO32 for ’short address accesses’
via VMEbus (A08 - A15 = CARD-ADDRESS)

3.3 Jumper Configuration

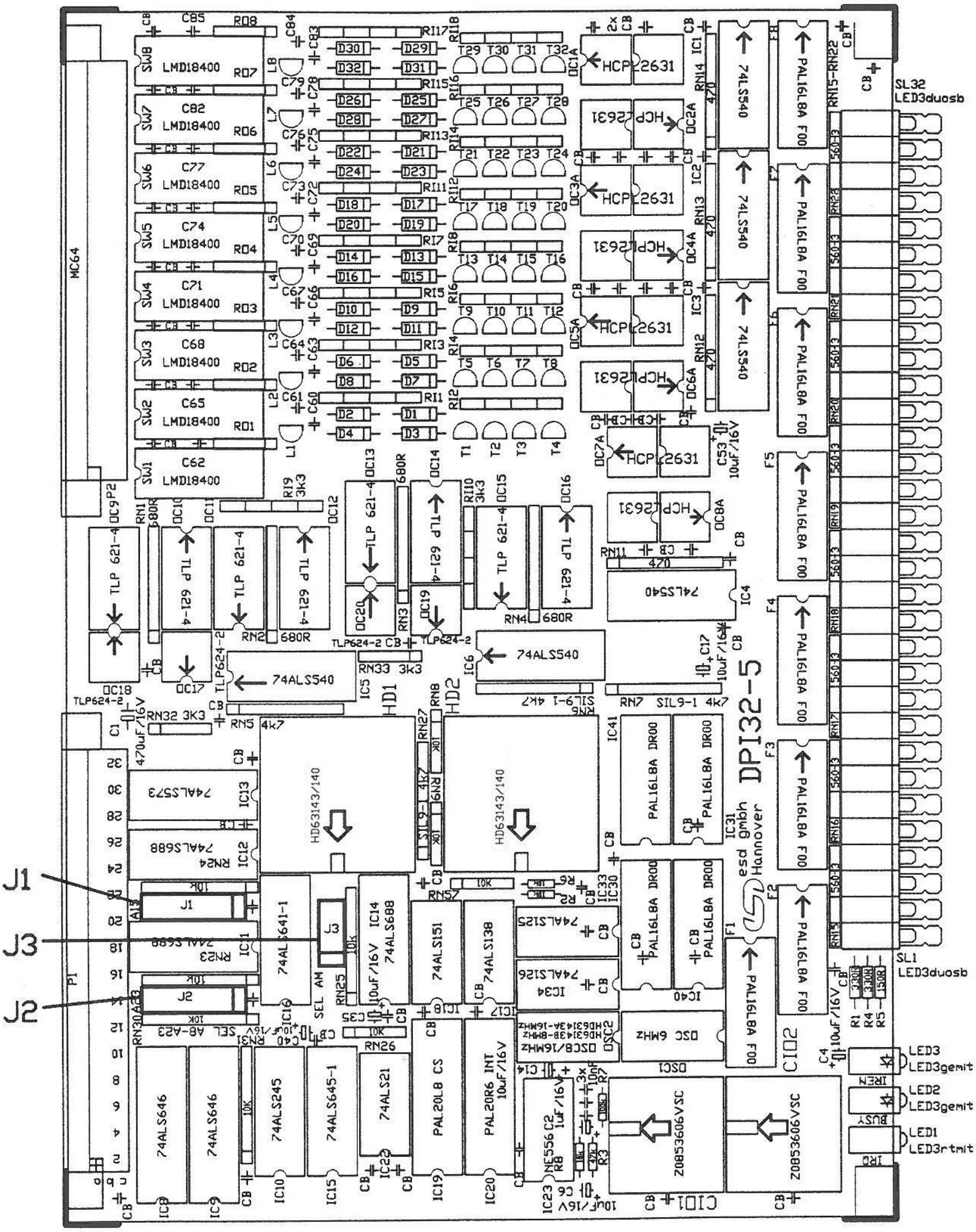


Figure 3: Jumper Position

3.3.1 Default Setting

The particular factory-settings (of the jumpers see following table) are marked in the table.
The jumpers configuration can be obtained from the insertion diagram. An inserted jumper corresponds to ’0’ (low) level of a signal.
In the following the jumpers are displayed in a position, as seen by the user, if he has the board lying in front of himself with the VMEbus connectors to the rear end.

Default jumper setting of jumpers J1 to J4:

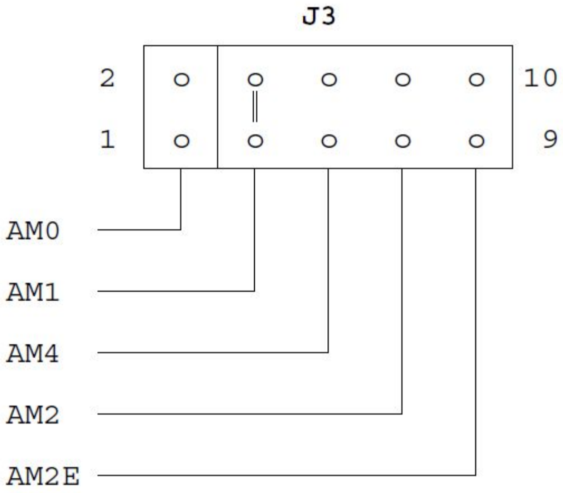
Jumper	Function	Setting
J1	basic address A08-A15	basic address of VME-DPIO32/63140 set to $xxE14000
J2	basic address A16-A23	
J3	address modifier	AM2 don’t care, i.e. access in the supervisory mode or user mode VME access A24/D16

Table 6: Default Jumper Setting

3.3.2 The Address-Modifier AM Jumper J3

The VME-DPIO32/63140 can be operated with access modes A24/D16 (standard) or A16/D16 (short).
At the default setting of jumpers displayed below A24/D16 accesses to the board are enabled. AM2 will be ignored, so user mode as well as supervisory mode can be used for addressing.

Default setting: Standard supervisory and non-privileged data access (A24-Mode)



The jumpers AM0, AM1 and AM4 are evaluated ’separately’. The jumpers AM2 and AM2E form a unit and are always evaluated together.

The jumpers AM0, AM1 and AM4 are evaluated as follows:

jumper/ pins	signal decoding	
	not inserted	inserted
AM0 1-2	1	0
AM1 2-3		
AM4 4-5		

Table 7: Evaluation of Jumpers AM0, AM1 and AM4

Permissible Positions of Jumpers AM2 and AM2E are as follows:

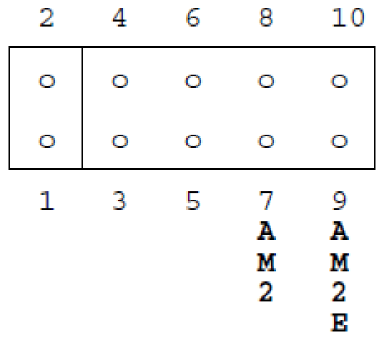
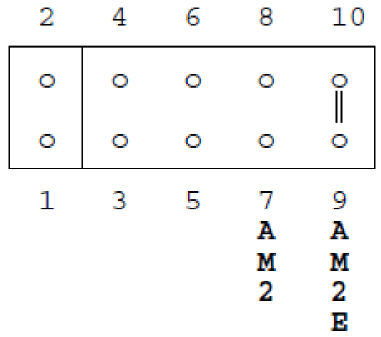
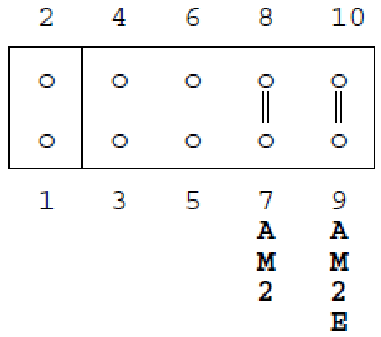
Position of jumpers AM2 and AM2E	evaluation
	AM2 = don't care
	AM2 = 1 (supervisory modes only)
	AM2 = 0 (non-privileged modes only)

Table 8: Permissible positions of jumpers AM2 and AM2E

Meaningful address modifier jumpers combinations for 24 accesses are recommended as follows:

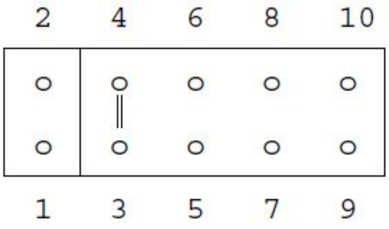
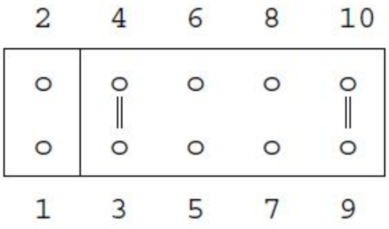
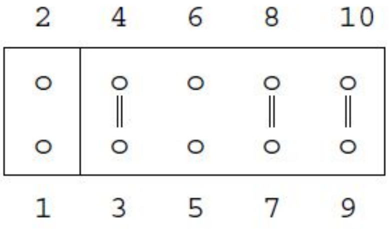
jumper J3	permissible AM codes		addressing mode
	AM5 AM4 AM3 AM2 AM1 AM0	HEX	
	1 1 1 0 0 1 1 1 1 1 0 1	39 3D	standard non-privileged data access or standard supervisory data access
	1 1 1 1 0 1	3D	standard supervisory data access
	1 1 1 0 0 1	39	standard non-privileged data access

Table 9: Recommended Access Modes for Standard Accesses (A24)

Meaningful address modifier jumpers combinations for 16 accesses are recommended as follows:

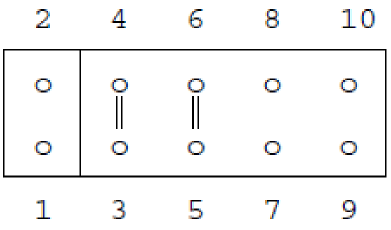
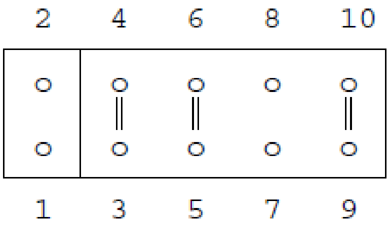
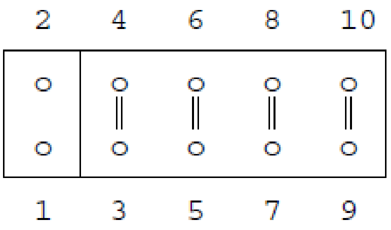
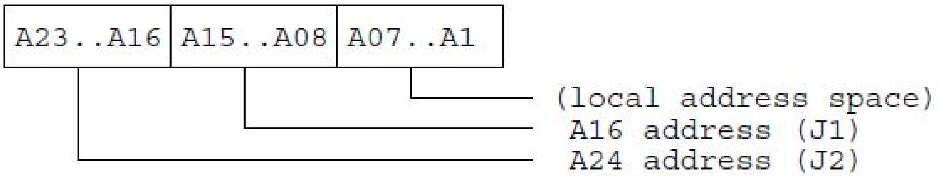
jumper J3	permissible AM codes		addressing mode
	AM5 AM4 AM3 AM2 AM1 AM0	HEX	
	1 0 1 0 0 1 1 0 1 1 0 1	29 2D	short non-privileged access or short supervisory access
	1 0 1 1 0 1	2D	short supervisory access
	1 1 1 0 0 1	29	short non-privileged access

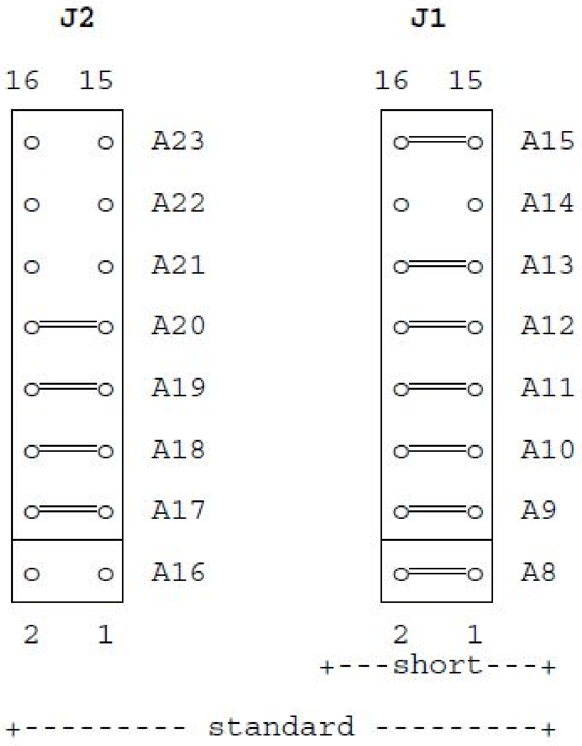
Table 10: Recommended Access Modes for Short Accesses (A16)

3.3.3 Basic Access Decoding via the Jumpers J1 and J2

The basic address of VME-DPIO32/63140 is set as follows:



Default setting = $E14000



An inserted jumper corresponds to the 'low' level of an address bit.

4. Interrupt Processing

The CIO Z8536 components CIO1 and CIO2 can generate an interrupt on a rising or falling edge of their input signals. The programming of the CIOs determines, at which edge the interrupt shall be generated.

The two local interrupt requests are combined in the interrupt logic.

The VMEbus interrupt disable and the VMEbus interrupt level are not programmable with the HD63140.
The VMEbus interrupt is always enabled. The level is hard wired to IRQ1, but can easily be changed to IRQ5 by soldering a wire bridge from IC17-pin 1 to IC17-pin 3 (74xx138).

If the HD63140 should trigger a VMEbus interrupt, a wire bridge is necessary
In the default configuration of the VME-DPIO32/63140 both HD63140 are not able to trigger an interrupt, because the multiplexer that chains the interrupt output of the controller to the CIO circuit input A7 is no longer controlled by the HD63140.
In the default configuration the CIO input A7 is always connected to connector P2 via the input circuit.

If it is necessary that a HD63140 triggers a VMEbus interrupt, the input port A7 of the CIO can be set by soldering a wire bridge between the following pins:

HD1: For the first HD63140 a wire bridge between pin 10 and pin 7 of IC33 (74xx125) has to be soldered. The bridge connects the interrupt line of the HD63140 to the port A7 of the CIO1 (Z8536).

HD2: For the second HD63140 a wire bridge between pin 13 and pin 7 of IC33 (74xx125) has to be soldered. The bridge connects the interrupt line of the HD63140 to the port A7 of the CIO2 (Z8536).

To execute each of the above listed modifications it is only necessary to solder additional wire bridges to the VME-DPIO32. It is not necessary to cut conductive paths at the PCB or to cut circuit pins.

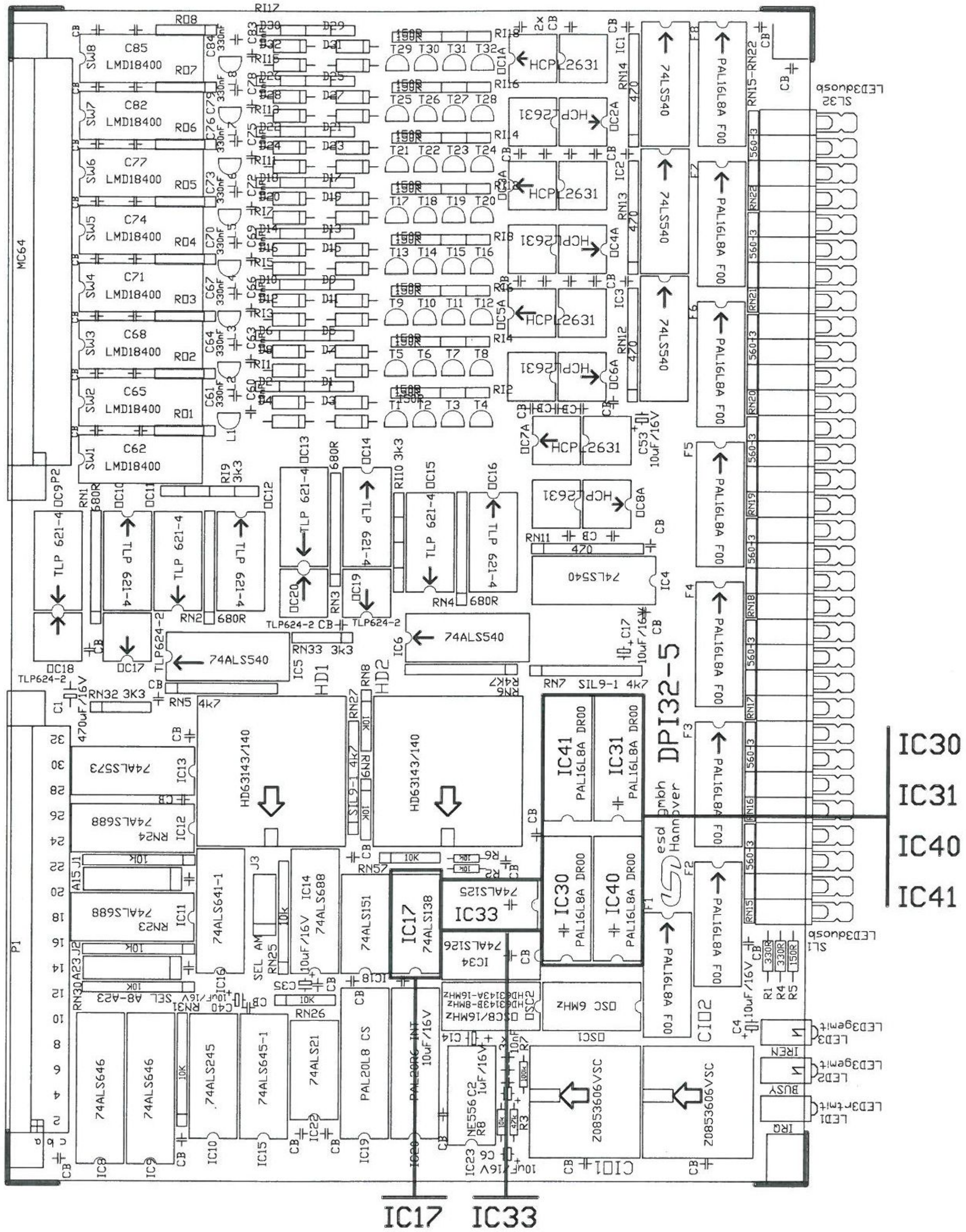


Figure 4: Position of circuits where wire bridges has to be added

5. Digital Inputs and Outputs

5.1 Controller Assignment to Inputs and Outputs

The VME-DPIO32/63140 is equipped with 4 controller components. The two CIO Z8536 controllers handle the digital inputs and together offer two timers/counters with a maximum input frequency of 3 MHz each.

Two HD63140 supply the digital outputs. The operating modes ’digital output’ or ’pulse width modulated output’ are possible. The HD63140 can also process input signals via multiplexers.
Moreover they make available a total of 16 counters with a maximum counter frequency of 100 kHz (duty cycle 1:1) each.
If the HD63140 controllers shall generate VMEbus interrupts, then their interrupt outputs are fed to the CIO Z8536 port A7. The interrupt handling on the VMEbus is processed via the CIO.

In the VME-DPIO32/63140 version the HD63140 controller is equipped instead of the HD63143 controller used in the older VME-DPIO32 versions.
If the HD63140 is equipped, some restrictions must be considered:

The I/O ports P40, P41, ...P46 and P50, P51, ...P55 are realized as digital input ports at the HD63143. At the HD63140 these ports are realized as analog inputs.
Therefore, **the I/O Ports can only be switched to input direction by hard wiring**

As before each channel of the VME-DPIO32/63140 can be configured as input or output.
There are only restrictions at the input operation of the HD63140 ports. (The following notes are with respect to the block diagram ‘Assignment of Inputs and Outputs to the Controllers’ at page 24 of this manual.)

A change of multiplexer direction can be achieved only by hard wiring, because the port pins P40 and P44 of the HD63143 that had controlled the multiplexer of the output ports of the HD63143 U0..U3 and U4..U7 are no longer available.

Without this wiring all HD63140 ports are switched to output mode, because the multiplexer control signals are connected to pull-ups. Each of the multiplexers IC30, IC40, IC31, IC41 (GAL16V8) can change the data direction of 4 channels.

Switching to input mode is done by connecting pin 11 of the multiplexers to ground. The ground potential is available e.g. at pin 10 of the multiplexer circuits.
The following table shows the assignment of the I/O channel to the multiplexer:

Channel	UPP Ports	Multiplexer Circuit
I/O1....I/O4	HD1: U0...U3	IC30
I/O5....I/O8	HD1: U4...U7	IC40
I/O17...I/O20	HD2: U0...U3	IC31
I/O21...I/O24	HD2: U4...U7	IC41

Figure 5 on page 25 displays the assignment of inputs and outputs on the VME-DPIO32 (With HD63143). The designations ’IN...’ and ’OUT...’ in column P2 display the input and output numbers, **where inputs and outputs with the same number physically cover the same pin on the P2 connector.**

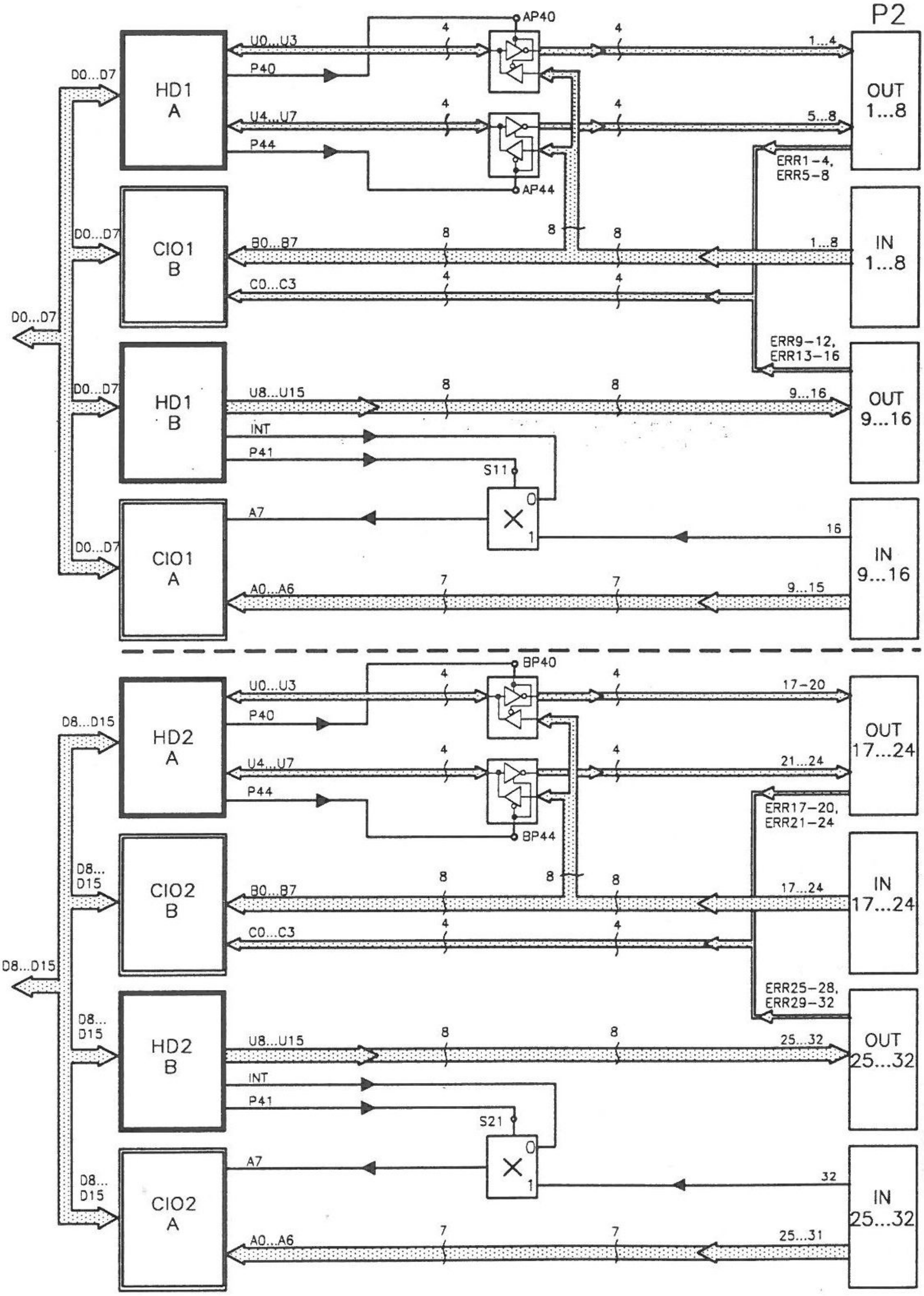


Figure 5: Assignment of Interrupts and Outputs to the Controllers (HD63143)

INFORMATION
Figure 5 shows the previous VME-DPIO32 version with HD63143. Please note that at the VME-DPIO32/63140 the I/O ports P40, P41, ...P46 and P50, P51, ...P55 can only be switched to input direction by hard wiring.

5.2 Pulse Processor HD63140 Structure

The HD63140 mainly consists of three functional units: The universal pulse processor, two serial interfaces and a RAM of 1024.
The serial interfaces are not used on the VME-DPIO32/63140. The HD63140 RAM is not available to the user in PCB version DPI32-5.

The internal pulse processor disposes of an own 16 bit wide ALU (Arithmetic Logic Unit).
The principal pulse processor function can be illustrated by a scheme, which builds up on a process table:
The HD63140 continuously runs the instructions of a process table, where up to 16 process descriptions can be listed. Each of these process descriptions contains informations (parameters) on a desired function.
These parameters contain e.g. the registers to be used, the used pins and functions assigned to the pins.
The following figure displays this construction again as a survey. A complete listing of all possible parameters can be obtained from the software description.

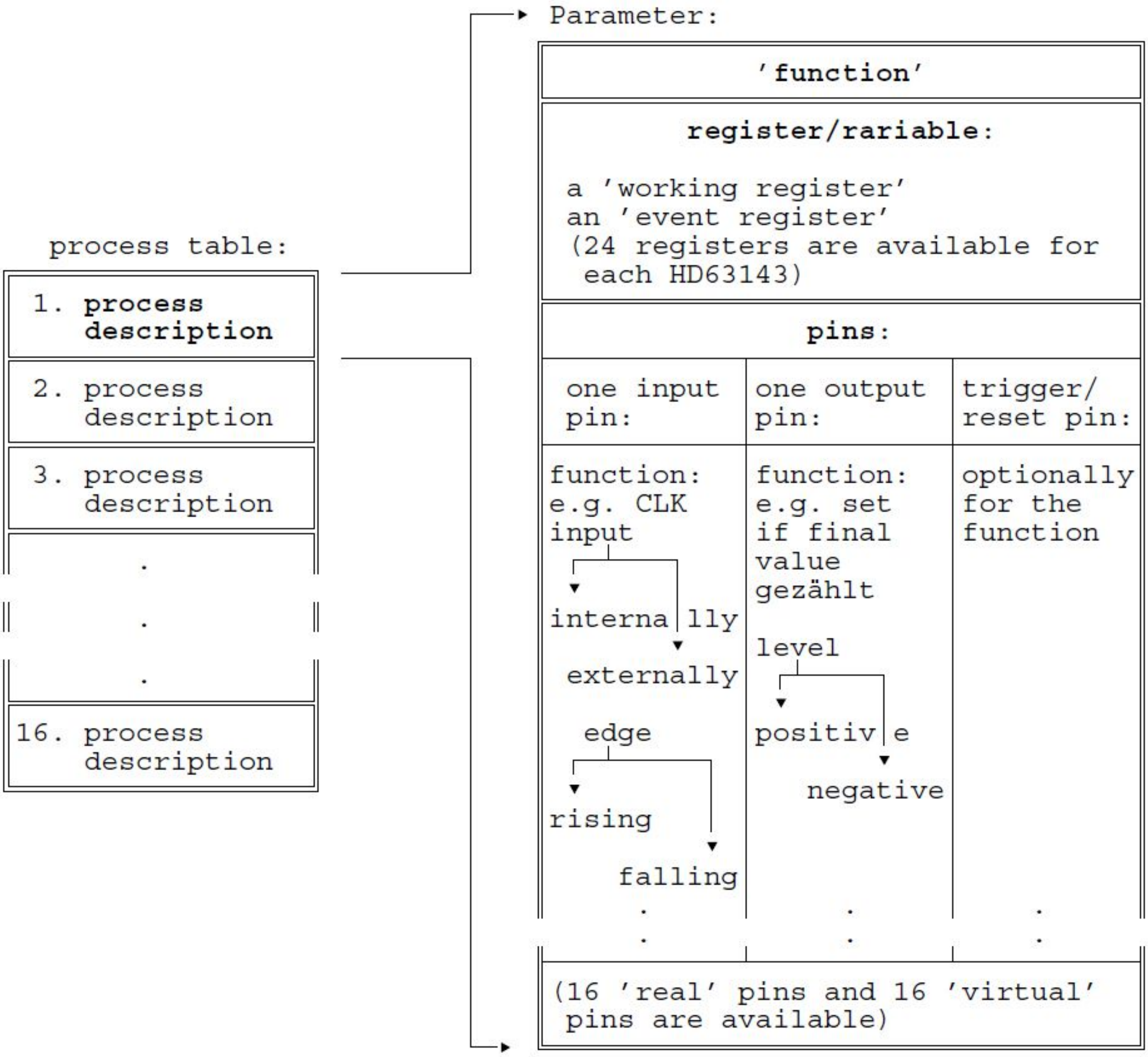


Figure 6: Functional Construction of HD63140

5.3 Input and Output Circuit of VME-DPIO32/63140

5.3.1 General

The VME-DPIO32/63140 is designed for 32 input or output channels. Each of the 32 channels can be operated either as input or output.
If a channel is operated as output, then the signal condition of the output can be read-back ’online’ via the input circuit, which is connected in parallel.
The channels are configured in groups of four, because each 4 outputs are supplied by one driver component. If a channel group shall operate as input group, all outputs of this group must be set to ’0’.
If at input operation of an I/O group no power supply is connected to the corresponding output driver, a part of the input current will flow into the output driver. In this case the input current consumption will increase. Thus it is recommended to connect a power supply to the output drivers of an I/O group as well when operating this group as inputs only.
The input voltage in this case may not exceed a maximum equal to U_{vccout} - 2V because otherwise the output drivers might be destroyed!

As output driver a LMD18400 is used. The driver component can connect voltages of 6V to 28V (HIGH level) to GND.
The output driver supply voltage must be supplied externally. Each 4 of 32 channels are connected to one voltage supply. With this, 8 different output groups, optoisolated from each other, are possible.
Each of the 8 output drivers disposes of an error output, which will be triggered on occurrence of an error at one or several channels.
The error outputs are connected to the C ports of the two CIO Z8536.

error signal of the outputs	at CIO/Port
1...4	CIO1/PC0
5...8	CIO1/PC1
9...12	CIO1/PC2
13...16	CIO1/PC3
17...20	CIO2/PC0
21...24	CIO2/PC1
25...28	CIO2/PC2
29...32	CIO2/PC3

Table 11: Connection of the Error Signals to the CIO Ports

An error output will be triggered at the following operating troubles:
- no load
- short-circuit to VCC or GND
- overvoltage
- overtemperature of the driver component

Comment to error handling:
If the error conditions ’overtemperature’ or ’supply voltage too high’ occur, the LMD18400 switches off all 4 outputs. If the error condition is no longer valid and the inputs of the driver are still active, the LMD18400 switches automatically the outputs on again.
The error condition ’unloaded output’ will not be detected: The outputs are connected to the inputs and therefore the outputs are continuously loaded with the small load of the input circuits.

5.3.2 Front Panel LEDs and Test Sockets

The channel status is displayed by two-coloured LEDs on the front panel:

LED display	meaning of the front panel LEDs at the various operating modes	
	channel = input	channel = output
LED OFF	no input signal	output signal = ’0’ and no error
LED GREEN	input active (’1’)	output signal = ’1’ and no error, or all outputs of this group (of four) are set to ’0’ and feeding at the output
LED RED	-	error condition occurred

Table 12: Meaning of the channel status LEDs on the front panel

Via a test socket on the front panel for each channel the input or the error signal can be controlled.

test socket plug connector	affect to the channels at the various operating modes	
	channel = input	channel = output
not inserted	applied input level will be read	occurring errors will be evaluated
inserted	input level will always be read as ’1’	occurring errors will be ignored

Table 13: Meaning of the channel status Test Sockets on the front panel

5.3.3 Input and Output Circuit Diagram

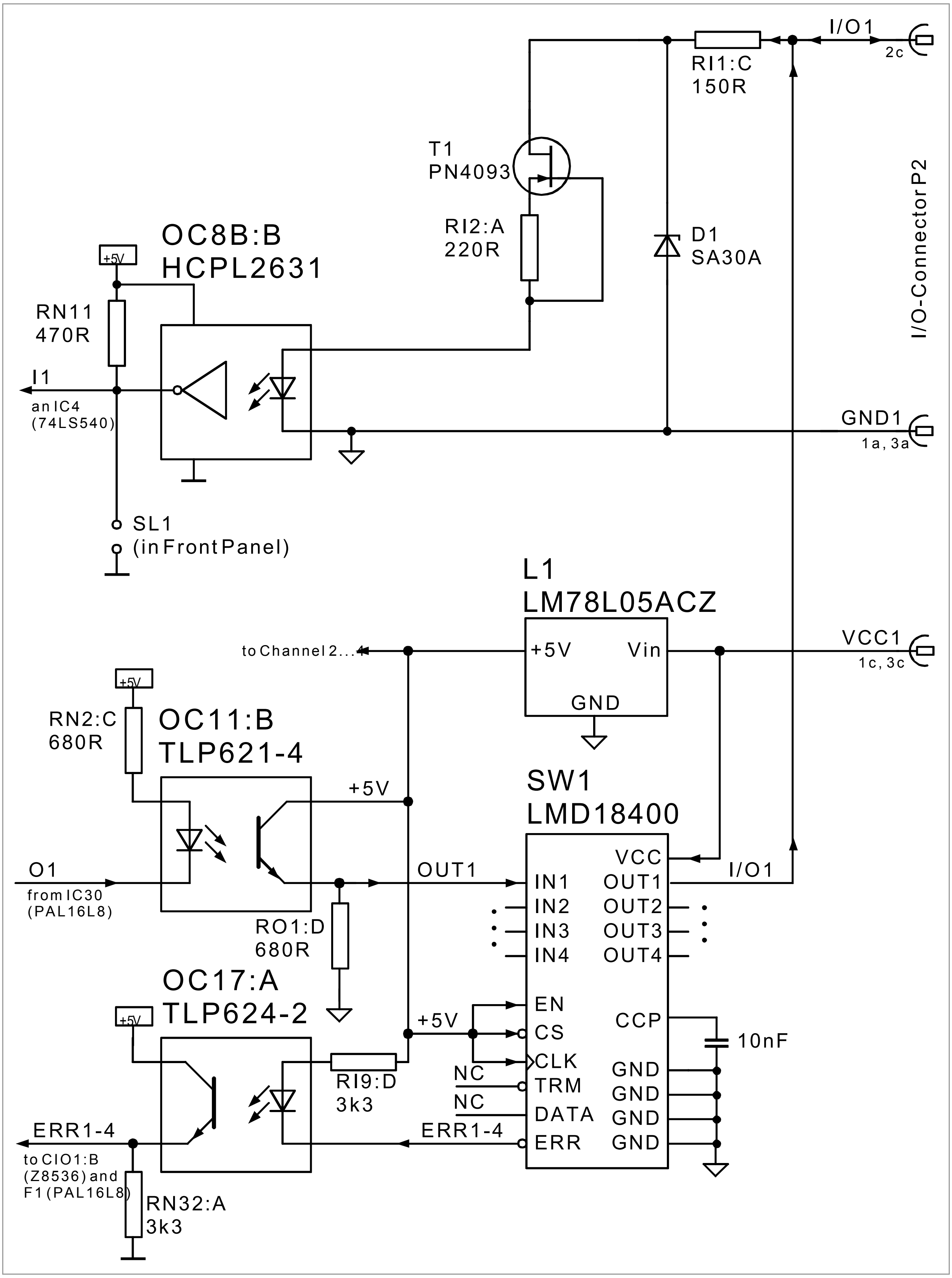


Figure 7: Input and output circuits (example: channel 1)

6. Hardware Installation

NOTICE
Read the safety instructions at the beginning of this document carefully, before you start with the hardware installation!

DANGER
Hazardous Voltage - **Risk of electric shock** due to unintentional contact with uninsulated live parts with high voltages inside of the system into which the VME-DPIO32/63140 is to be integrated.
→ Disconnect all hazardous voltages (mains voltage) before opening the system.
→ Ensure the absence of voltage before starting any electrical work

NOTICE
Electrostatic discharges may cause damage to electronic components.

→ To avoid this, please discharge the static electricity from your body by touching the metal case of the VMEbus system *before* you touch the VME-DPIO32/63140.
→ Furthermore, you should prevent your clothes from touching the VME-DPIO32/63140, because your clothes might be electrostatically charged as well.

Procedure:

1. Switch off your VMEbus system and all connected peripheral devices (monitor, printer, etc.).
2. Discharge your body as described above.
3. If necessary, configure the jumpers as described in chapter “Jumper Configuration” from page 15.
4. Disconnect the VMEbus system from the mains.

   DANGER
   Hazardous Voltage
   Risk of electric shock due to unintentional contact with uninsulated live parts with high voltages.

   → Disconnect all hazardous voltages (mains voltage) before opening the system.
   → If the system does not have a flexible mains cable, but is directly connected to mains, disconnect the power supply via the safety fuse and make sure that the fuse cannot switch on again unintentionally (i.e. with caution label).

5. Open the case if necessary.
6. Insert the VME-DPIO32/63140 board into the selected slot. Carefully push the board until it snaps into place.
7. Close the system's case again.
8. Connect the system to mains again (mains connector or safety fuse).
9. Switch on the system and the peripheral devices. - End of hardware installation.

7. Connector Pin Assigments

7.1 VMEbus P1

pin	row a	row b	row c
1	DATA 0	-	DATA 8
2	DATA 1	-	DATA 9
3	DATA 2	-	DATA 10
4	DATA 3	BG0 IN*]	DATA 11
5	DATA 4	BG0 OUT*]	DATA 12
6	DATA 5	BG1 IN*]	DATA 13
7	DATA 6	BG1 OUT*]	DATA 14
8	DATA 7	BG2 IN*]	DATA 15
9	GND	BG2 OUT*]	GND
10	-	BG3 IN*]	-
11	GND	BG3 OUT*]	-
12	DS1*	-	SYSRESET*
13	DS0*	-	LWORD*
14	WRITE*	-	AM5
15	GND	-	ADDR 23
16	DTACK*	AM0	ADDR 22
17	GND	AM1	ADDR 21
18	AS*	AM2	ADDR 20
19	GND	AM3	ADDR 19
20	IACK*	GND	ADDR 18
21	IACKIN*	-	ADDR 17
22	IACKOUT*	-	ADDR 16
23	AM4	GND	ADDR 15
24	ADDR 7	IRQ7*	ADDR 14
25	ADDR 6	IRQ6*	ADDR 13
26	ADDR 5	IRQ5*	ADDR 12
27	ADDR 4	IRQ4*	ADDR 11
28	ADDR 3	IRQ3*	ADDR 10
29	ADDR 2	IRQ2*	ADDR 9
30	ADDR 1	IRQ1*	ADDR 8
31	-	-	-
32	+ 5V	+ 5V	+ 5V

P1 connector according to DIN 41 612-C 96 / a+b+c

Signals with * : active low
Current rating : max 1.0 A per pin

- .... pin is not connected on the PCB

] .... signals are connected on the PCB

7.2 I/O Connector P2

pin	row a	row c
1	GND1	VCC1
2	I/O2	I/O1
3	GND1	VCC1
4	I/O4	I/O3
5	GND2	VCC2
6	I/O6	I/O5
7	GND2	VCC2
8	I/O8	I/O7
9	GND3	VCC3
10	I/O10	I/O9
11	GND3	VCC3
12	I/O12	I/O11
13	GND4	VCC4
14	I/O14	I/O13
15	GND4	VCC4
16	I/O16	I/O15
17	GND5	VCC5
18	I/O18	I/O17
19	GND5	VCC5
20	I/O20	I/O19
21	GND6	VCC6
22	I/O22	I/O21
23	GND6	VCC6
24	I/O24	I/O23
25	GND7	VCC7
26	I/O26	I/O25
27	GND7	VCC7
28	I/O28	I/O27
29	GND8	VCC8
30	I/O30	I/O29
31	GND8	VCC8
32	I/O32	I/O31

P1 connector according to DIN 41 612-C 96 / a+c

Signal Description

GNDx, VCCx … power supply (U_{vcc}) for the digital I/O circuits to be fed externally. Each 4 channels are locally connected to the same power supply (x = 1, 2,...,8)

I/Ox ... I/O channels of VME-DPIO32/63140.
(x = 1, 2, ..., 32)

7.3 Terminal Block I/O Connector P2 Phoenix FLKM64 or FLKMS64

pin	row a	pin	row c
2	GND1	1	VCC1
4	I/O2	3	I/O1
6	GND1	5	VCC1
8	I/O4	7	I/O3
10	GND2	9	VCC2
12	I/O6	11	I/O5
14	GND2	13	VCC2
16	I/O8	15	I/O7
18	GND3	17	VCC3
20	I/O10	19	I/O9
22	GND3	21	VCC3
24	I/O12	23	I/O11
26	GND4	25	VCC4
28	I/O14	27	I/O13
30	GND4	29	VCC4
32	I/O16	31	I/O15
34	GND5	33	VCC5
36	I/O18	35	I/O17
38	GND5	37	VCC5
40	I/O20	39	I/O19
42	GND6	41	VCC6
44	I/O22	43	I/O21
46	GND6	45	VCC6
48	I/O24	47	I/O23
50	GND7	49	VCC7
52	I/O26	51	I/O25
54	GND7	53	VCC7
56	I/O28	55	I/O27
58	GND8	57	VCC8
60	I/O30	59	I/O29
62	GND8	61	VCC8
64	I/O32	63	I/O31

Signal Description

GNDx, VCCx … power supply (Uvcc) for the digital I/O circuits to be fed externally. Each 4 channels are locally connected to the same power supply (x = 1, 2,...,8)

I/Ox ... I/O channels of VME-DPIO32, (x = 1, 2, ..., 32)

7.4 Wiring Diagram

System						
VME-DPIO32 Page 1	No. 32 input or output channels		□ 5 (6) V	□ 12 V		□ 24 V channel 1 - 8
- Digital Input/Output			Wago/ Phoenix	INTERNAL		
designation	Channel	Pol	Terminal	P2 Pin		Signal
				a	c	
external supply required (only if channel 1 ... 4 are outputs)	-	+ ⊥	1 2	1	1	VCC GND
	1	+ ⊥	3 2	1	2	I/O1 GND
	2	+ ⊥	4 2	2 1		I/O2 GND
external supply required (only if channel 1 ... 4 are outputs)	-	+ ⊥	5 6	3	3	VCC GND
	3	+ ⊥	7 6	3	4	I/O3 GND
	4	+ ⊥	8 6	4 3		I/O4 GND
external supply required (only if channel 5 ... 8 are outputs)	-	+ ⊥	9 10	5	5	VCC GND
	5	+ ⊥	11 10	5	6	I/O5 GND
	6	+ ⊥	12 10	6 5		I/O6 GND
external supply required (only if channel 5 ... 8 are outputs)	-	+ ⊥	13 14	7	7	VCC GND
	7	+ ⊥	15 14	7	8	I/O7 GND
	8	+ ⊥	16 14	8 7		I/O8 GND

System						
VME-DPIO32	No.		□ 5 (6) V		□ 12 V	□ 24 V
Page 2	32 input or output channels				channel 9 - 16	
- Digital Input/Output			Wago/ Phoenix	INTERNAL		
designation	Channel	Pol	Terminal	P2 Pin a	 c	Signal
external supply required (only if channel 9 ... 12 are outputs)	-	+ ⊥	17 18	 9	9	VCC GND
	9	+ ⊥	19 18	 9	10	I/O9 GND
	10	+ ⊥	20 18	10 9		I/O10 GND
external supply required (only if channel 9 ... 12 are outputs)	-	+ ⊥	21 22	 11	11	VCC GND
	11	+ ⊥	23 22	 11	12	I/O11 GND
	12	+ ⊥	24 22	12 11		I/O12 GND
external supply required (only if channel 13 ... 16 are outputs)	-	+ ⊥	25 26	 13	13	VCC GND
	13	+ ⊥	27 26	 13	14	I/O13 GND
	14	+ ⊥	28 26	14 13		I/O14 GND
external supply required (only if channel 13 ... 16 are outputs)	-	+ ⊥	29 30	 15	15	VCC GND
	15	+ ⊥	31 30	 15	16	I/O15 GND
	16	+ ⊥	32 30	16 15		I/O16 GND

System						
VME-DPIO32 Page 3	No. 32 input or output channels		□ 5 (6) V	□ 12 V		□ 24 V channel 17 - 24
- Digital Input/Output			Wago/ Phoenix	INTERNAL		
designation	Channel	Pol	Terminal	P2 Pin a	 c	Signal
external supply required (only if channel 17 ... 20 are outputs)	-	+ ⊥	33 34	17	17	VCC GND
	17	+ ⊥	35 34	17	18	I/O17 GND
	18	+ ⊥	36 34	18 17		I/O18 GND
external supply required (only if channel 17 ... 20 are outputs)	-	+ ⊥	37 38	19	19	VCC GND
	19	+ ⊥	39 38	19	20	I/O19 GND
	20	+ ⊥	40 38	20 19		I/O20 GND
external supply required (only if channel 21 ... 24 are outputs)	-	+ ⊥	41 42	21	21	VCC GND
	21	+ ⊥	43 42	21	22	I/O21 GND
	22	+ ⊥	44 42	22 21		I/O22 GND
external supply required (only if channel 21 ... 24 are outputs)	-	+ ⊥	45 46	23	23	VCC GND
	23	+ ⊥	47 46	23	24	I/O23 GND
	24	+ ⊥	48 46	24 23		I/O24 GND

System			
VME-DPIO32	No.	□ 5 (6) V	□ 12 V □ 24 V
Page 4	32 input or output channels		channel 25 - 32

- Digital Input/Output			Wago/ Phoenix	INTERNAL		
designation	Channel	Pol	Terminal	P2 Pin		Signal
				a	c	
external supply required (only if channel 25 ... 28 are outputs)	-	+ ⊥	49 50	25	25	VCC GND
	25	+ ⊥	51 50	25	26	I/O25 GND
	26	+ ⊥	52 50	26 25		I/O26 GND
external supply required (only if channel 25 ... 28 are outputs)	-	+ ⊥	53 54	27	27	VCC GND
	27	+ ⊥	55 54	27	28	I/O27 GND
	28	+ ⊥	56 54	28 27		I/O28 GND
external supply required (only if channel 28 ... 32 are outputs)	-	+ ⊥	57 58	29	29	VCC GND
	29	+ ⊥	59 58	29	30	I/O29 GND
	30	+ ⊥	60 58	30 29		I/O30 GND
external supply required (only if channel 28 ... 32 are outputs)	-	+ ⊥	61 62	31	31	VCC GND
	31	+ ⊥	63 62	31	32	I/O31 GND
	32	+ ⊥	64 62	32 31		I/O32 GND

8. Order Information

Type	Properties	Order No.
VME-DPIO32/63140	32 digital input or output, Timer, optical isolation, no routing from I/O to UPP63140, (RoHS except HD63140)	V.1607.04
Accessories		
VME-P2-ADAPT1	64-pole adapter block for P2 with screw terminal blocks, ribbon cable included	V.1923.01
VME-P2-ADAPT2	64-pole adapter block for P2 with clamp terminal blocks, ribbon cable included	V.1923.02
VME-DPIO32-P2VCC	output power connection to P2 via 6,3 mm flat-connectors, separately for the 8 output groups of one VME-DPIO32/63140	V.1607.90
VME-DPIO32-P2VCC-3X	combined output power connection to 3x P2 via 6,3 mm flat-connectors for all output groups of three VME-DPIO32/63140	V.1607.93
Software		
VME-DPI32-OS9	C driver for OS-9 as source code	P.1607.50
VME-DPI32-VxW	C driver for VxWorks as source code	P.1607.56

For detailed information about the driver availability for your special operating system, please contact our sales team.

Table 14: Order information

PDF Manuals
For availability of English manuals see table below.
Please download the manuals as PDF documents from our esd website www.esd.eu for free.

Manuals		Order No.
VME-DPIO32/63140-ME	Hardware manual and Software manual in English	V.1607.21

Table 15: Available manuals

Printed Manuals
If you need a printout of the manual additionally, please contact our sales team: sales@esd.eu for a quotation. Printed manuals may be ordered for a fee.

VME - DPIO32

32 digital Inputs or Outputs

Software Manual

NOTE

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Manual File:	I:\TEXTE\DOKU\MANUALS\VME\DPIO32\ENGLISCH\DPIO21S.EN6
Date of Print:	29.07.97

Described Software:	`dpisrv 2.7`

Changes in the chapters

The changes in the user's manual listed below affect changes in the software, as well as changes in the description of the facts only.

Alternations in the appendix versus previous revisions	Alternations in software	Alternations in documentation
First english manual issue.	-	-

Inhalt

Seite

1. Overview

The construction of the Universal Pulse Processor (UPP) HD63143 has already been described in the hardware manual, where also the states for the assignment of inputs and outputs have been explained in detail.

This software description deals with the realization of UPP functions in RTOS/PEARL.

The firmware provides the user with various entries for the operation of the DPIO32. Below, the entries are assigned to the operating modes 'pin I/O' and 'pulse processing mode' (PPM). The entries may overlap at assignment (as, e.g., for the interrupt handling).

Pin I/O means all 'simple' level changes of input and output pins and contains the input operation of the channels and the handling of error messages at output channels.

In the pulse processing mode all counting functions of the HD63143 will be explained.

Following tables give an overview of the implemented entries:

Pin I/O	
`SEND...SETDP1`	Enabling an output of the first DPIO32 in the system
`SEND...SETDP2`	Enabling an output of the second DPIO32 in the system
`SEND...RESDP1`	Disabling an output of the first DPIO32 in the system
`SEND...RESDP2`	Disabling an output of the second DPIO32 in the system
`SEND...OUTDP1`	Setting all outputs of the first DPIO32 in the system
`SEND...OUTDP2`	Setting all outputs of the second DPIO32 in the system
`TAKE...ERRDP1`	Reading the error status of the output driver of the LMD18400
`TAKE...GETDP1`	Reading the entries or error flags of the first DPIO32 in the system
`TAKE...GETDP2`	Reading the entries or error flags of the second DPIO32 in the system

Overview

Interrupt Handling	
`CALL IRQDP1`	Setting the interrupt mode of the CIO Z8635 entries
`CALL EVDP1`	Assignment of EVENTs to the CIO Z8536 entries
`CALL IRQUP1`	Setting the interrupt mode of the HD63143 entries
`CALL IRSUPL`	Determining the pin which triggered the interrupt - lower UPP
`CALL IRSUPH`	Determining the pin which triggered the interrupt - upper UPP
`CALL LEVDP1`	Setting the board_interrupt_level on the VMEbus

Pulse Processing Mode	
`CALL UPPINI`	Resetting the HD63143 and determining the maximum function number
`CALL MODDPI`	Pin assignment and operating modes of the HD63143
`CALL SUPDPI`	Setting the HD-pulse register
`value=GUPDPI`	Reading the HD-pulse register

Table 1.1.1: Overview of the available entries

The entries SETDP2, RESDP2, OUTDP2 and GETDP2 access the second DPIO32 in the system. The VMEbus basis address of the second DPIO32 has to be set to $xxE14100 (an offset of +$100 to the first DPIO32). The explanation of how to set the basis address can be taken from the hardware manual.

2. Entries for the Pin-I/O Operation (Setting and Reading Inputs or Outputs)

2.1 Selection and Assignment of Inputs and Outputs

For a better understanding of how to assign inputs and outputs in the DPIO32, please consult the figure 'Assignment of inputs and outputs to the controllers' , which can be found in the hardware manual.
In this chapter the assignment of inputs and outputs for pin-I/O operation, that is for 'quasistatical' circuits, will be described.
The pin assignment for UPP functions (timer/counter) will be explained in the following chapter 'Entries for the Pulse Processing Mode'.

2.1.1 Pin-I/O Entries

All 32 channels of the DPIO32 can always be read transparently as entries via the CIOs Z8536.

This function works independently from the use of channels as outputs by the UPPs HD63143. If this were the case, only the output level would be played back and of course no external input signals must be applied!

At the same time channels 1...8 and 17...24 can be used in groups of four as inputs of the HD63143. Doing this, however, only UPP functions are possible, because the pin-I/O input operation is run via the CIOs. As mentioned before, the UPP function will be explained in the following chapter 'Entries for the Pulse Processing Mode'.

2.1.2 Pin-I/O Outputs

In order to run a channel as statical output the following has to be noticed:

A pin can only work as a pin-I/O output, if it was selected for the UPP mode 'pin I/O' and the complete group of four which is part of it is defined as output in the mode.

As soon as a channel of a group of four was defined as UPP input, the multiplexer will enable all four pins as inputs!

After a power-on or RESET all 32 pins of the RTOS/PEARL firmware included in the range of delivery are set to mode 'pin I/O' and are defined as output pins.

Pin I/O Mode

2.2 Enabling Individual Outputs - `SETDP1, SETDP2`

Declaration:

```
SPC SETDP1 DATION OUT BASIC GLOBAL;
SPC SETDP2 DATION OUT BASIC GLOBAL;
```

Variable definition:

```
DCL setbit_no1 FIXED;
DCL setbit_no2 FIXED;
```

Value range:

setbit_no1,
setbit_no2 : 1...32 (real pins)
33...40 (hidden pins lower HDC (HD1))
41...48 (hidden pins upper HDC (HD2))
(For more detailed informations about the pin types, refer chapter 4.)

Procedure call:

```
SEND setbit_no1 TO SETDP1
```

```
SEND setbit_no2 TO SETDP2
```

The output with the according channel number is being enabled.

The selection `SETDP1` sets the output of the first DPIO32 in the system and the selection `SETDP2` sets an output on the second DPIO32 (if available).

2.3 Disabling Individual Outputs - `RESDP1, RESDP2`

Declaration:

```
SPC RESDP1 DATION OUT BASIC GLOBAL;
SPC RESDP2 DATION OUT BASIC GLOBAL;
```

Variable definition:

```
DCL resbit_no1 FIXED;
DCL resbit_no2 FIXED;
```

Value range:

resbit_no1,
resbit_no2 : 1...32 (real pins)
33...40 (hidden pins lower HDC (HD1))
41...48 (hidden pins upper HDC (HD2))
(For more detailed informations about the pin types, refer chapter 4.)

Procedure call:

```
SEND resbit_no1 TO RESDP1
```

```
SEND resbit_no2 TO RESDP2
```

The output with the according channel number is being disabled.

The call `RESDP1` sets the output on the first DPIO32 in the system and the call `RESDP2` sets an output on the second DPIO32 (if available).

Pin I/O Mode

2.4 Setting All Outputs - `OUTDP1, OUTDP2`

By means of the DATIONs `OUTDP1` and `OUTDP2` it is possible to set and play back (the physical) outputs. The declaration in &Problemteil therefore has to be as follows:

```
SPC OUTDP1 DATION INOUT BASIC GLOBAL;
SPC OUTDP2 DATION INOUT BASIC GLOBAL;
```

Variable definition:

```
DCL obit321 BIT(32);
DCL obit322 BIT(32);
```

Value range:

```
obit321,
obit322 :  $00000000...$FFFFFFFF (channel no.)
```

Procedure call:

```
SEND obit321  TO OUTDP1;
```

```
SEND obit322  TO OUTDP2;
```

All outputs are set accordingly to the selected DATION and the specified variable.

```
Output e.g.:   $00000001 --▸ only output  1 is active
               $80000000 --▸ only output 32 is active
```

Selection `OUTDP1` responds to the outputs on the first DPIO32 and selection `OUTDP2` responds to the outputs on the second DPIO32 (if available).

2.5 Reading the Error Status of the Outputs - **ERRDP1**

The DATION `ERRDP1` shows the error status of the output drivers. For a group of four outputs a shared error signal is generated.

```
SPC ERRDP1 DATION IN BASIC GLOBAL;
```

Variable definition:

```
DCL error BIT(32);
```

Value range:

error: For each channel group four bits are returned which are always set similiarly, because each driver has only one error output for four channels. If the four bits are set to '0000', no error occurred. If the bits are set to '1111', an error occurred in at least one channel.

Bit	31...28	27...24	23...20	19...16	15...12	11...8	7...4	3...0
Channel	32...29	28...25	24...21	20...17	16...13	12...9	8...5	4...1

Notes on error recovery:

If the error states 'excess temperature' or 'supply voltage too high' occur, the LMD18400 disables its four outputs. If the error state removes and the inputs of the driver component are still active, the LMD18400 automatically enables the outputs again!

Procedure call:

```
TAKE error FROM ERRDP1;
```

Pin I/O Mode

2.6 Reading the Inputs or the Actual Value of the Output -GETDP1, GETDP2

Declaration:

```
SPC GETDP1 DATION IN BASIC GLOBAL;
SPC GETDP2 DATION IN BASIC GLOBAL;
```

Variable definitions:

```
DCL ibit321 BIT(32);
DCL ibit322 BIT(32);
```

Value ranges:

```
ibit321,
ibit322 :  $00000000...$FFFFFFFF
```

Procedure calls:

```
TAKE ibit321 FROM GETDP1
```

```
TAKE ibit322 FROM GETDP2
```

All entries are read or played back.

GETDP1 accesses the first DPIO32 board in the system, GETDP2 accesses the second DPIO32 (if available).

e.g.: $00000001 --► only input 1 is active or output 1 is enabled
$80000000 --► only input 32 is active or output 32 is enabled

3. Interrupt Handling

The inputs of both CIOs Z8536 or the inputs of both UPPs HD63143 can be configurated as interrupt sources on the DPIO32.
The CIOs are directly connected to the local interrupt logic. The HD63143 can trigger an interrupt, because its interrupt output can be applied to a CIO input via multiplexers (see hardware manual DPIO32, figure 'Assignment of Inputs and Outputs to the Controllers'). The input channels used for this are channel 16 and channel 32. If the HD63143 are to trigger interrupts, these inputs cannot be used for external signals anymore!

The entries for the configuration of CIO-Z8536 interrupts and HD63143 interrupts are constructed largely independently from each other. They use, however, the same parameters for the assignment of EVENTs to the pins. Therefore, always the last entry made for this pin is valid!

3.1 Setting the Interrupt Modes of the CIO Z8536 Inputs - `IRQDP1`

This function sets the interrupt mode for the 32 inputs guided to the CIOs Z8536.

Declaration:

```
SPC IRQDP1 ENTRY (FIXED, FIXED) GLOBAL;
```

Variable definition:

```
DCL (irpin, irmode) FIXED;
```

Value ranges:

irpin : Number of input channel:
0 ...no channel selected
1...32 ...input channel of the DPIO32
Attention: The interrupt mode of pins 16 and 32 can also be changed later via function `IRQUP1`!

irmode: Interrupt mode:
0 ...no interrupt
1 ...interrupt at rising edge
2 ...interrupt at falling edge
3 ...pulse mode: interrupt at rising edge
4 ...pulse mode: interrupt at falling edge
5 ...pulse mode: interrupt at rising and falling edge

Procedure call:

```
CALL IRQDP1 (irpin, irmode)
```

Interrupt Handling

In modes 1 and 2 pulses which are received during interrupt handling are not recognized. The interrupt handling lasts about 10 µs.

The advantage of modes 3 to 5 is that a pulse which is received during an interrupt handling is recognized. If several pulses are received during that time, however, only the pulse with the highest priority is recognized by the CIO Z8536.

The entry with the highest number has the highest and the entry with the lowest number the lowest priority (example: A7 -▸ highest priority, A0 -▸ lowest priority).

Note: As soon as the interrupt mode 'pulse mode' is set for a pin of a CIO-Z8536 input group (8 inputs), all other pins of this group are also in the pulse mode!

After a RESET following EVENTs are standardly assigned to the CIO inputs:

Interrupt at entry no.	EVENT
1	`EV00000001`
2	`EV00000002`
3	`EV00000004`
:	:
31	`EV40000000`
32	`EV80000000`

Table 3.1.1: Assignment of triggered EVENTs to the channels

This assignment can be changed by means of procedure `EVTDP1`, described below.

3.2 Assignment of EVENTs to the CIO Z8536 Inputs - EVTDP1

By means of this procedure it is possible to change the default setting of the assignment of EVENTs to the CIO-Z8536 inputs of the DPIO32. Moreover, there is the possibility to assign several EVENTs to one pin.

Declaration:

```
SPC EVTDP1 ENTRY (FIXED, BIT(32)) GLOBAL;
```

Variable definition:

```
DCL evpin FIXED;
DCL event BIT(32);
```

Value ranges:

evpin : Number of the input channel:

0 ...no channel selected

1...32 ...input channel of the DPIO32

Attention: The EVENT assignment of pins 16 and 32 can also be changed later via the `IRQUP1` function!

event: $00000000...$FFFFFFFF

Procedure call:

```
CALL EVTDP1 (evpin, event)
```

Example: The EVENTs 1 and 32 are to be triggered for pin 3 at fulfilled interrupt condition (according to IRQDP1).

The parameters have to be set like this:

```
evpin =  3
event = $80000001
```

3.3 Setting the Interrupt Mode of the HD63143 Pins - `IRQUP1`

This function sets the interrupt mode for the 48 possible HD63143 pins of the DPIO32. It contains the 'real' and the 'hidden' pins of both HD63143 controllers.

An HD63143 can trigger an interrupt, if a defined edge is determined at one of its 24 pins. The initiating signal can, for instance, be applied externally to a pin defined as input or the signal can be set as output of a UPP function.

The edges which are triggering an interrupt are determined in the HD63143 and cannot be changed. Following table shows the assignments of pins and edges. The second line shows the original pin designation of the HD63143 data sheet. The third and fourth line specify the pins which are to be transmitted, if the RTOS/PEARL firmware is used for the DPIO32.

Interrupt at edge	↓								↑				↓				↑				↓			
UPP no.	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Pin no. on lower HD (HD1)	40	39	38	37	36	35	34	33	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Pin no. on upper HD (HD2)	48	47	46	45	44	43	42	41	32	31	29	28	27	26	25	24	23	22	21	20	19	18	17	16

Table 3.3.1: Interrupt-initiating edges of the HD63143 pins on the DPIO32

If the procedure is called, it overwrites the interrupt configurations possibly made via `IRQDP1` and `EVTDP1` for the input channel 16 (lower UPP) or channel 32 (upper UPP). On the other hand the functions `IRQDP1` and `EVTDP1` would change the settings of IRQUP1, if they would be selected later for channels 16 or 32!

Declaration:

```
SPC IRQUP1 ENTRY (FIXED, FIXED, BIT(32)) GLOBAL;
```

Variable definition:

```
DCL (irqpin, irqmode, eventmask) FIXED;
```

Value ranges:

`irqpin` : Number of the input channel:
0 ...no channel selected
1...16 ...'real' pin on lower UPP
17...32 ...'real' pin on upper UPP
33...40 ...'hidden' pin on lower UPP
41...48 ...'hidden' pin on upper UPP

Note: Concerning the circuit the UPP pins 9...16 or 25...32 are wired as outputs at P2. They still can be used as input pins, if they are set by another process. **For these UPP pins it isn't possible to apply an external input signal to P2!** If these pins are required as inputs they can be used as pin-I/O inputs of the CIO Z8536 (UPP functions are not possible).

`irqmode`: Interrupt mode:
0 ...no interrupt
1 ...interrupt released

`eventmask`: EVENT mask:
By means of this BIT(32) variable one or more EVENTs are selected for the specified pin. These EVENTs are triggered at fulfilled interrupt condition.

`$00000000...$FFFFFFFF`

Attention: By selecting this function the interrupt performance of the input channels 16 and 32 applied to the CIO Z8536 is automatically configurated again. All previous settings, such as via `IRQDP1` or `EVTDP1` are lost.

Procedure call:

```
CALL IRQUP1 (irqpin, irqmode, eventmask)
```

3.4 Determining HD63143 Pins Which Triggered an Interrupt - IRSUPL, IRSUPH

After the initiation of an EVENT it is necessary to find out by which pin it was triggerd, because it isn't possible to determine an EVENT for each of the 48 UPP pins. These DATIONs show all pins of the HD63143 which have changed since the last selection of this DATION.

Declaration:

```
SPC IRSUPL DATION INOUT BASIC GLOBAL;
SPC IRSUPH DATION INOUT BASIC GLOBAL;
```

Variable definition:

```
DCL (pin_l, pin_h) BIT(32);
```

Value ranges:

pin_l,
pin_h: Pins whose level has changed since the last selection.
`$00000000...$000FFFFF`

e.g.: `$00000010` -> pin 5

Procedure calls:

```
TAKE pin_l FROM IRSUPL
```

```
TAKE pin_h FROM IRSUPH
```

3.5 Setting the Board-Interrupt Level on the VMEbus - LEVDP1

Declaration:

```
SPC LEVDP1 ENTRY (FIXED) GLOBAL;
```

Variable definition:

```
DCL irlev FIXED;
```

Value ranges:

irlev : Interrupt release and interrupt level
0 ...interrupt locked
1...7 ...VMEbus-interrupt level

Procedure call:

```
CALL LEVDP1 (irlev)
```

4. Entries for the Pulse Processing Mode

4.1 Register Structure and I/O Pins

The pulse processor of the HD63143 requires various I/O pins for its operating modes (trigger pin, gate pin, clock pin,...). These pins can either be 'real' or 'virtual' pins.
Real pins are physically available input or output pins of the controllers. The pin numbers of the real pins are chosen in such a way that they correspond to the channel-designation numbers on connector P2.

Attention!
It has to be secured that the pin direction chosen in the software is identical to the direction of the connected signals!

A pin which is only available as an output pin can nevertheless be used as an input pin (of another process) in the controller at the same time. Of course it isn't possible to apply an external input signal at the connector for this pin!

Directly after a hardware RESET all UPP pins are defined as input. The output multiplexers are enabled for output operation, however, in order to set the outputs (channels 1...8, 17...24) at P2 of the DPIO32 to '0' and activate the front LEDs in connection with internal pull-down resistors.
Immediately after a RESET the RTOS/PEARL firmware, included in the delivery range, defines the UPP pins as output pins. Now they can be activated as outputs in pin-I/O operation.

The output multiplexers enable the input operation as soon as a pin of the port nibble (1...4, 5...8 or 17...20, 21...24) has been defined as input. For the output operation of a nibble it is therefore necessary to define all four pins as outputs. If one group is defined as input, the front LEDs can luminesce, but the the outputs themselves remain inactive.

The virtual pins are only available internally of the HD63143 controllers. They are differentiated into 'hidden pins' and 'dummy pins' again. Hidden pins can be set and read. They are evaluable for further functions. Dummy pins should be used, if a pin has to be specified according to the rules of the operating modes, but is not required for further functions anymore.

Pins are assigned to every process to be handled. Within an HD63143 controller it is possible to use the pins of one process in any other process. It is possible, for instance, to define the output pin of one process as input pin of another process.

Pulse Processing Mode

Apart from the pins registers are assigned to each process. The HD63143 manages its registers similiarly to the functional pins in a 'register pool'. Within an HD63143 the register of one process, e.g., whose content is always incremented, can serve as limit value of the counting cycle of another process.

4.2 Resetting the HD63143 and Determining the Maximum Function No. -`UPPINI`

This call executes following procedures:

1. The maximum function no. is transmitted.
   It determines the length of the function table to be handled and therefore has direct influence onto the resolution of the counting functions.

> The time T_{RESOL} specified in the following table shows the minimum possible pulse time for the high and low pulse for the inputs. That means that the maximum possible countable frequency is $f_{MAX} < [1/(2x\ T_{RESOL})]$ at a pulse duty factor of 1:1.
> For the outputs T_{RESOL} determines the minimum possible period time. This is not valid, however, for signals which are to be externally accessible via the connector P2, because those signals are transmitted via the output drivers LMD18400. The output drivers can generally only enable pulses of ≥ 10 µs!

2. All UPP ports are set to bit-I/O mode.

3. The UPP is disabled.

(After a RESET the UPP is also preset, as described under points 2 and 3.)

Declaration:

```
SPC UPPINI ENTRY (FIXED, FIXED, FIXED) GLOBAL;
```

Variable definition:

```
DCL cardno FIXED;
DCL devno  FIXED;
DCL mfnr   FIXED;
```

Value ranges:

`cardno:` Card no.
Number of the DPIO32 board in the VMEbus system. If the system contains only one board, a '1' is specified, here.
1...n ...board 1 to n

`devno:` Device no.
By means of this parameter the two UPPs of one board are differentiated.
1 ...lower UPP (HD1)
2 ...upper UPP (HD2)

`mfnr` : Maximum function number

`mfnr`	Number of procedures to be executed	max. resolution T_{RESOL} [µs]
0	16	8,00
1	0	0,25
2	1	0,50
3	2	0,75
4	3	1,00
5	4	1,25
6	4	1,50
7	5	1,75
8	6	2,00
9	7	2,25
10	8	2,50
11	8	2,75
12	9	3,00
13	10	3,25
14	11	3,50
15	12	3,75
16	12	4,00
17	13	4,25
18	14	4,50
19	15	4,75
20	16	5,00
21	16	5,25
22	16	5,50
23	16	5,75
24	16	6,00
25	16	6,25
26	16	6,50
27	16	6,75
28	16	7,00
29	16	7,25
30	16	7,50
31	16	7,75
(32)	16	8,00

Table 4.2.1: Meaning of the maximum function number (`mfnr`)

Procedure call:

```
CALL UPPINI (cardno, devno, mfnr)
```

4.3 Pin Assignment and Operating Modes of the HD63143 -`MODDPI`

By means of this entry the pulse processors of the two HD63143 are initialized. The desired functions are assigned to the 'real' and 'virtual' pins and the operating mode of the processor is selected. Furthermore the registers required for the operating modes are assigned.

> **Attention!**
> During the selection of `MODDPI` the pulse processor is stopped, that means that new initialisations are to be avoided during operation! Parameter defaults via `SUPDPI`, however, are transparently (see also entry `SUPDPI`).

Declaration:

```
SPC MODDP1 ENTRY (FIXED,FIXED,FIXED,FIXED,FIXED,FIXED,FIXED,FIXED,
                  FIXED,FIXED,FIXED,FIXED,FIXED) GLOBAL;
```

Variable definition:

```
DCL (crd,op,opol,ip,iedg,tp,tedg,gp,mode,fnr,wr,ar,prld) FIXED;
```

Value range:
The value ranges of the parameters will be explained in detail below.

Procedure call:

```
CALL MODDPI(crd,op,opol,ip,iedg,tp,tedg,gp,mode,fnr,wr,ar,prld)
```

4.3.1 Selection of DPIO32 Board, of Pins and Edges

`crd` **: Card No. (if a system contains more than one DPIO32)**
0 ...ignore board
1...16 ...board 1 to 16

op : **Selection of output pins**

64 different pins can be selected:

Pin no. to be entered op =	Pin type	Pin designation of the two HD63143 controllers
0	no pin	-
1...16 1*)	output pin ('real')	1...16 lower HDC (HD1)
17...32 2*)		1...16 upper HDC (HD2)
33...40	hidden pin ('virtual')	17...24 lower HDC (HD1)
41...48		17...24 upper HDC (HD2)
49...56	dummy pin ('virtual')	25...32 lower HDC (HD1)
57...64		25...32 upper HDC (HD2)

1)* The numbers to be entered of the real pins have been selected in a way that they match the channel designation numbers on the connector P2.

Pins 9...16 or 25...32 are wired as outputs at P2. The I/O circuit of pins 1...8 or 17...24 can be programmed in groups as four either as output circuit or input circuit.

Table 4.3.1: Selection of output pins in PPM operation

It has to be taken care of that the pin direction of the real pins selected in the software corrsponds to the connected signals!

opol: Polarity of output signals

0 ...output is 'LOW active'
1 ...output is 'HIGH active'

ip: Selection of input pins

48 different pins can be selected:

Pin no. to be entered *ip* =	Pin type	Pin designation of the two HD63143 controllers
0	internal cycle T = 5µs	-
1...16 1*) 17...32 2*)	input pin ('real')	1...16 lower HDC (HD1) 1...16 upper HDC (HD2)
33...40 41...48	hidden pin ('virtual')	17...24 lower HDC (HD1) 17...24 upper HDC (HD2)

1)* The numbers to be entered of the real pins have been selected in a way that they match the channel designation numbers on the connector P2.

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**

The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

Table 4.3.2: Selection of input pins in PPM operation

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

iedg: Selection of the active edge of the input signal

0 ...input function locked
1 ...rising edge active
2 ...falling edge active
3 ...rising and falling edge active

`tp`: Selection of trigger pins

48 different pins can be selected:

Pin no. to be entered `tp` =	Pin type	Pin designation of the two HD63143 controllers
0	internal cycle T = 5µs	-
1...16 1*) 17...32 2*)	input pin ('real')	1...16 lower HDC (HD1) 1...16 upper HDC (HD2)
33...40 41...48	hidden pin ('virtual')	17...24 lower HDC (HD1) 17...24 upper HDC (HD2)

1)* The numbers to be entered of the real pins have been selected in a way that they match the channel designation numbers on the connector P2.

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**

The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

Table 4.3.3: Selection of trigger pins in PPM operation

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

`tedg`: Selection of the active edge of the trigger signal

0 ...input function locked
1 ...rising edge active
2 ...falling edge active
3 ...rising and falling edge active

gp: Selection of gate pins

48 different pins can be selected:

Pin no. to be entered `tp` =	Pin type	Pin designation of the two HD63143 controllers
0	internal cycle T = 5µs	-
1...16 1*) 17...32 2*)	input pin ('real')	1...16 lower HDC (HD1) 1...16 upper HDC (HD2)
33...40 41...48	hidden pin ('virtual')	17...24 lower HDC (HD1) 17...24 upper HDC (HD2)

1)* The numbers to be entered of the real pins have been selected in a way that they match the channel designation numbers on the connector P2.

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**

The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

Table 4.3.4: Selection of gate pins in PPM operation

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

4.3.2 Selection of the Pulse Processing Mode by Parameter ***mode***

***mode*: Selection of the pulse processing mode**

Starting from firmware version `dpisrv 2.5` following operating modes are implemented:

mode	Name	Short description
0	Pin I/O	only static setting and reading without counting functions
1	NOP	no operation on pulse mode
2	INC	increment counter, pulse out
3	FFC	fifty-fifty duty cycle counter with compare
4	PWC	pulse width counter, reset by trigger pulse, PWM-output
5	GTS	gated counter with sample
6	UDS	up/down counter with sample
7	TPC	two phase up-down counter
8	FRS	free running counter/timer with sampling
9	INS	interval counter/timer with sampling
10	FRC	free running counter/timer with compare
11	OSC	one shot counter/timer with compare
12	GTC	gated counter/timer with compare
13	CTO	combination trigger one shot counter/timer
14	SIT	shift input (serial in)
15	SOT	shift output (serial out)
16	SPO	shift parallel output

If 100 (decimal) are added to the parameter value by *mode*, the counting direction of the working register turns, that means the working register (*wr*) is not counted up but counted down instead!

The various modes will be described in more detail below. Furthermore the useful value range of other parameters of `MODDPI` is specified for every operating mode.

4.3.3 Pin-I/O Operation

The pin-I/O operation has to be selected for pins which are not to be set by counting functions, but 'quasi statically' via the entries `SETDP1`, `RESDP1` or `OUTDP1`. In this mode counting functions are not possible.

The static read-in of channels via `GETDP1` is, independent from the selected UPP mode, always possible (also if the pin-I/O mode had not been selected for the according pin).

After a RESET the firmware sets all channels to pin-I/O operation, defines all real UPP pins as outputs and sets them to '0'.

The other paramaters of `MODDPI` have to be set as follows if this mode is chosen:

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
PinI/O	1-16	1*)	0	1*)	0	0	0	0	0	0	0	0	0

1*) For the pin-I/O operation only the use of real pins is useful: Pin no. 1-16 (HD1) or 17-32 (HD2)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**

The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

4.3.4 NOP - no operation on pulse mode

No procedures are executed.

In this operating mode the other parameters of `MODDPI` are set as follows:

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
NOP	1-16	0	0	0	0	0	0	0	1	1-32	0	0	0

The parameters ***fnr***, ***wr***, ***ar***, and ***prld*** will be explained in detail after parameter ***mode***.

Pulse Processing Mode

4.3.5 INC - increment counter, pulse Out

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
`INC`	`1-16`	`1*)`	`0/1`	`2*)`	`0-3`	`0`	`0`	`0`	`2`	`1-32`	`1-48`	`1-48`	`MAX*`

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

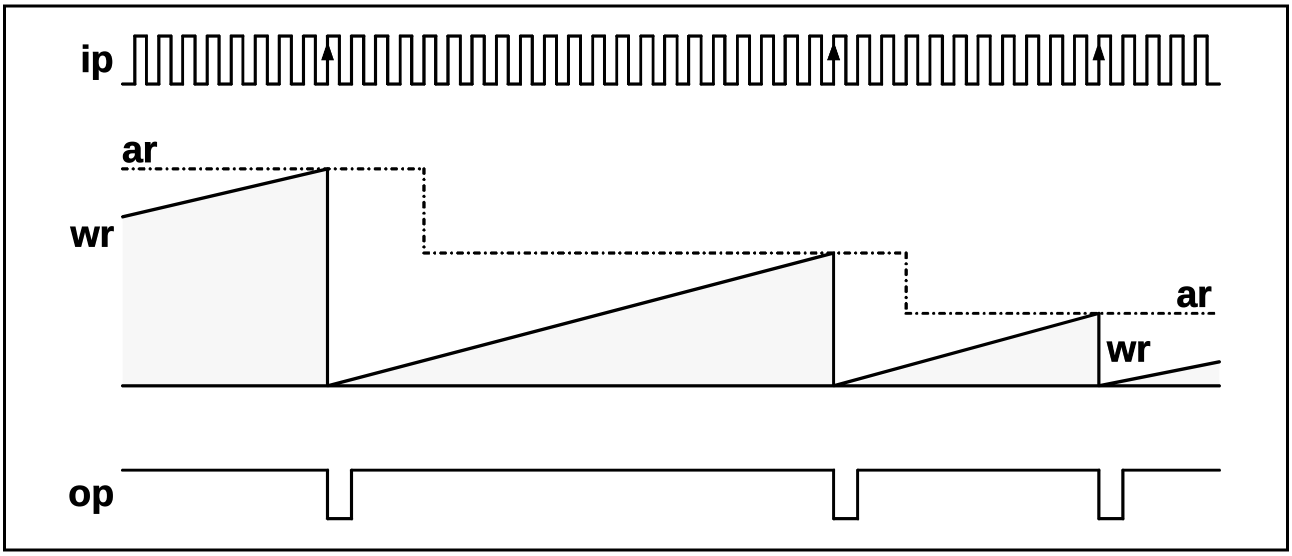
1*) As ouput pins either 'real' or 'hidden' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

2*) The input pin can be assigned with the same pin types as the output pin. In addition the internal cycle can serve as an input (*ip*=0).

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

`MAX*` Final value of the counter by means of which the auxiliary and the working registers are loaded.



Further parameters not shown:
`opol = 0`
`iedg = 1`
`tp   = 0`

Fig. 4.3.1: Timing example for the INC operation

Setting condition for the output pin: *op* := *wr* ≥ *ar*

The auxilary register (*ar*) is only changed by the CPU.

4.3.6 FFC - fifty-fifty duty cycle counter with compare

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
FFC	1-16	1*)	0/1	2*)	0-3	0	0	0	3	1-32	1-48	1-48	MAX*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

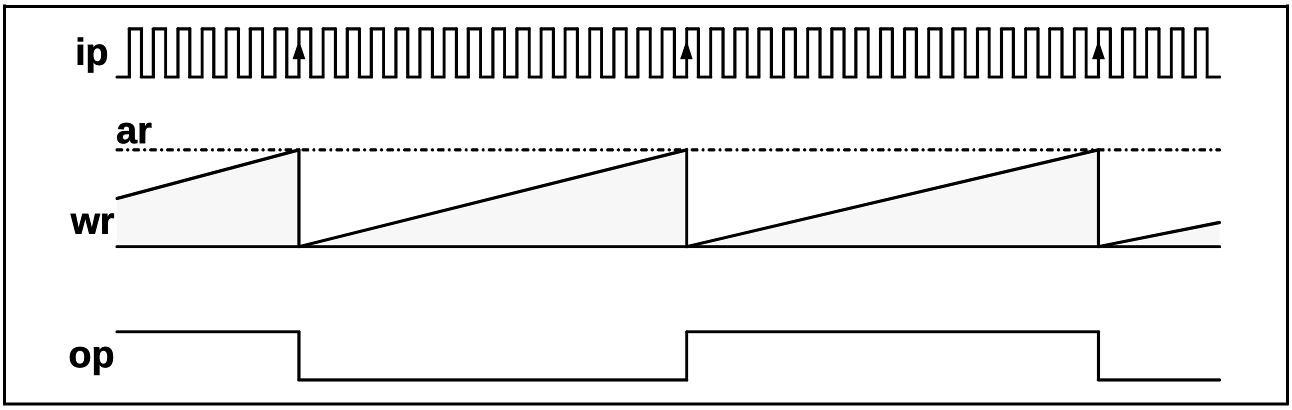
1*) As ouput pins either 'real' or 'hidden' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

2*) The input pin can be assigned with the same pin types as the output pin. In addition the internal cycle can serve as an input (*ip*=0).

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

MAX* Final value of the counter by means of which the auxiliary and the working registers are loaded.



Further parameters not shown:
opol = 0
iedg = 1
tp = 0

Fig. 4.3.2: Timing example for the FFC operation

The output pin changes its level when reaching the setting condition.

Setting condition for the output pin: $op := wr \geq ar$

Pulse Processing Mode

4.3.7 PWC - pulse width counter, reset by trigger pulse

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
PWC	1-16	1*)	0/1	2*)	0-3	3*)	0-3	0	4	1-32	1-48	1-48	MAX*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter `mode`.

1*) As ouput pins either 'real' or 'hidden' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)

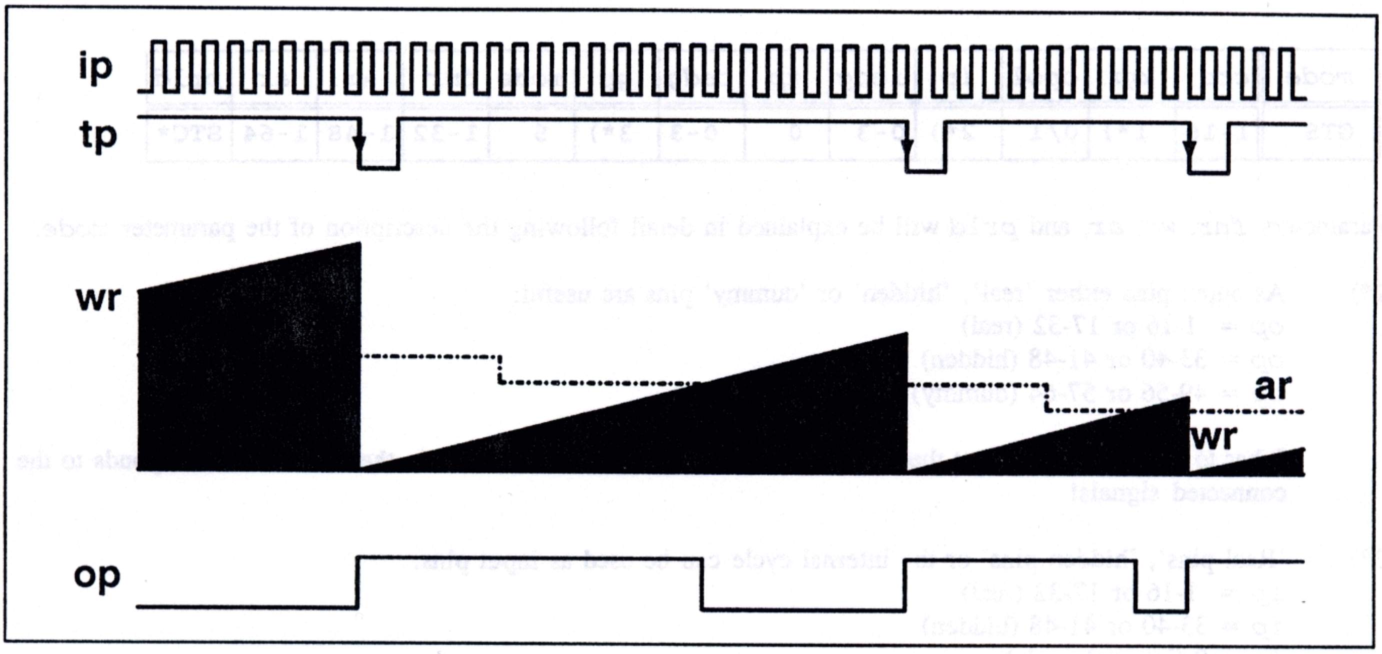
It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

2*) The input pin can be assigned with the same pin types as the output pin. In addition the internal cycle can serve as an input (*ip*=0).

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) For the trigger pin the same conditions apply as for the input pin.

MAX* Final value of counter by means of which the auxiliary anbd working register are loaded.



Further parameters not shown:
opol = 0
tedg = 2

Fig. 4.3.3: Timing example for the PWC operation

Setting condition for the output pin: *op* := *wr* ≤ *ar*
By means of the trigger pin the working register (*wr*) is reset.

The following circuit diagram gives an example for the combination of various processes in order to generate a pulsewidth-modulated output signal.

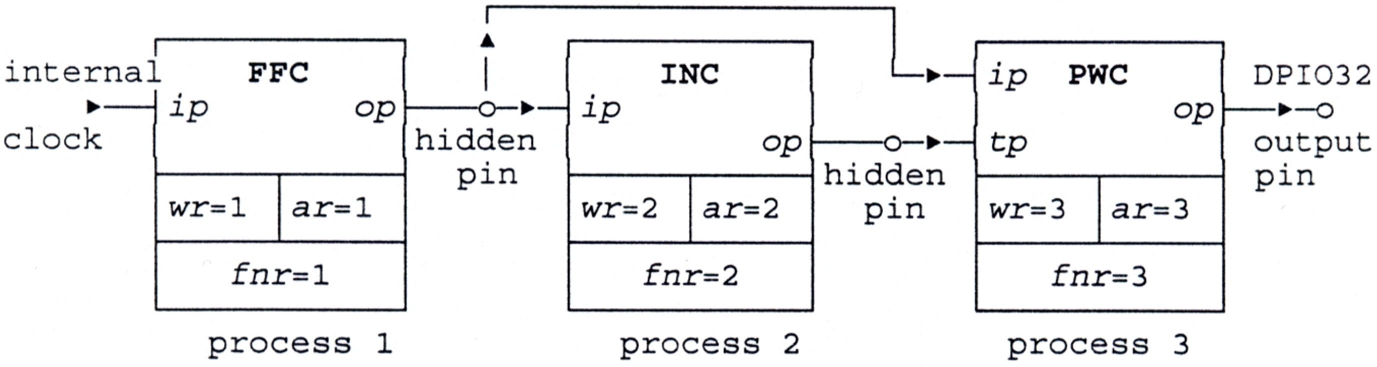


Fig. 4.3.4: Example for the generation of a PWM output signal

Pulse Processing Mode

4.3.8 GTS - gated counter with sample

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
GTS	1-16	1*)	0/1	2*)	0-3	0	0-3	3*)	5	1-32	1-48	1-64	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) As ouput pins either 'real', 'hidden' or 'dummy' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)
op = 49-56 or 57-64 (dummy)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

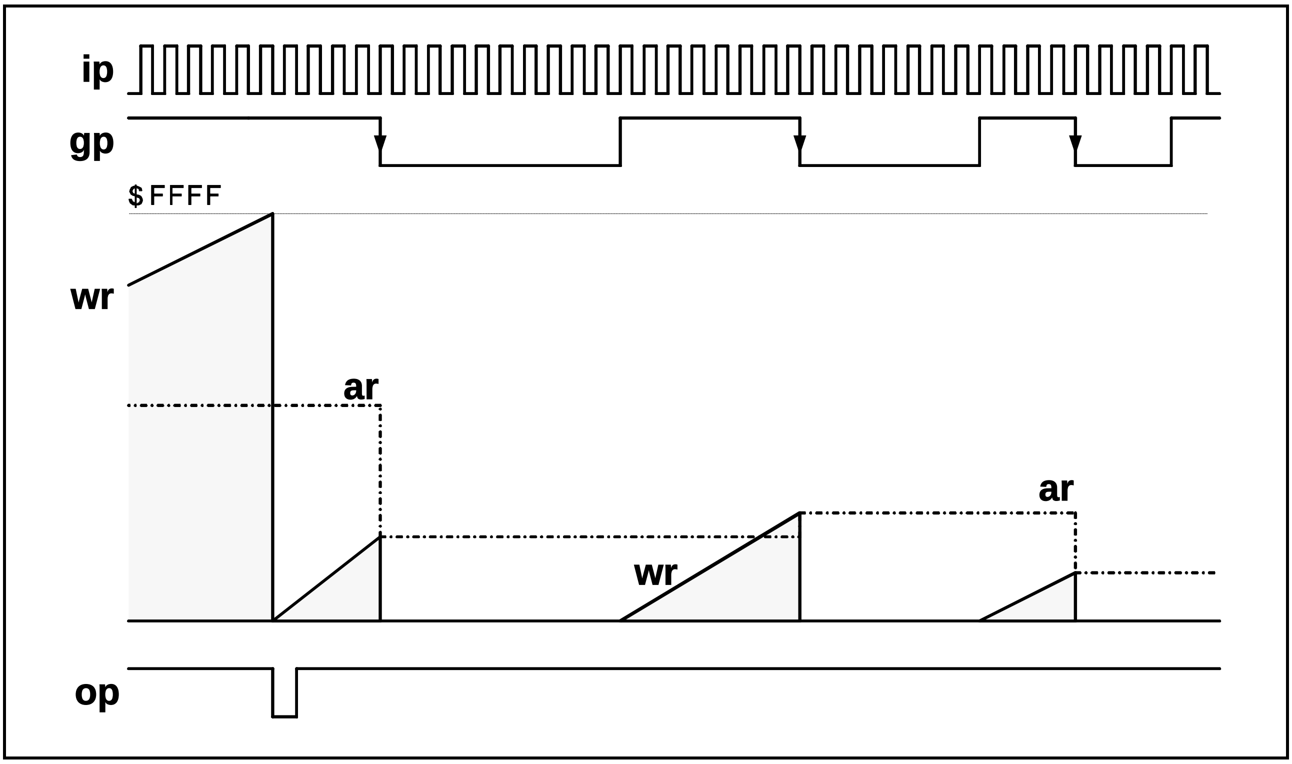
2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As gate pins 'real' or 'hidden pins' are possible:
gp = 1-16 or 17-32 (real)
gp = 33-40 or 41-48 (hidden)
gp = 0 (no gate pin)

Otherwise the same conditions apply for gate pin and input pin.

STC* Value with which the auxiliary and the working register are preloaded after the procedure call.



Further parameters not shown:
`opol` = 1
`tedg` = 2

Fig. 4.3.5: Timing example for GTS operation

By means of the gate pin's (`gp`) active edge, which is determined by `tedg`, the actual value of the working register (`wr`) is taken over into the auxiliary register (`ar`) and the `wr` is reset.
The active status of the gate input in which the `wr` is incremented is selected by means of parameter '`opol`'!

The output pin is only being set, if the maximum value of the counter ($FFFF) is reached.

The output pin (`op`) and the `ar` can be of 'dummy' type.

Pulse Processing Mode

4.3.9 UDS - up/down counter with sample

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
UDS	1-16	1*)	0/1	2*)	0-3	3*)	0-3	4*)	6	1-32	1-48	1-64	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) As ouput pins either 'real', 'hidden' or 'dummy' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)
op = 49-56 or 57-64 (dummy)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

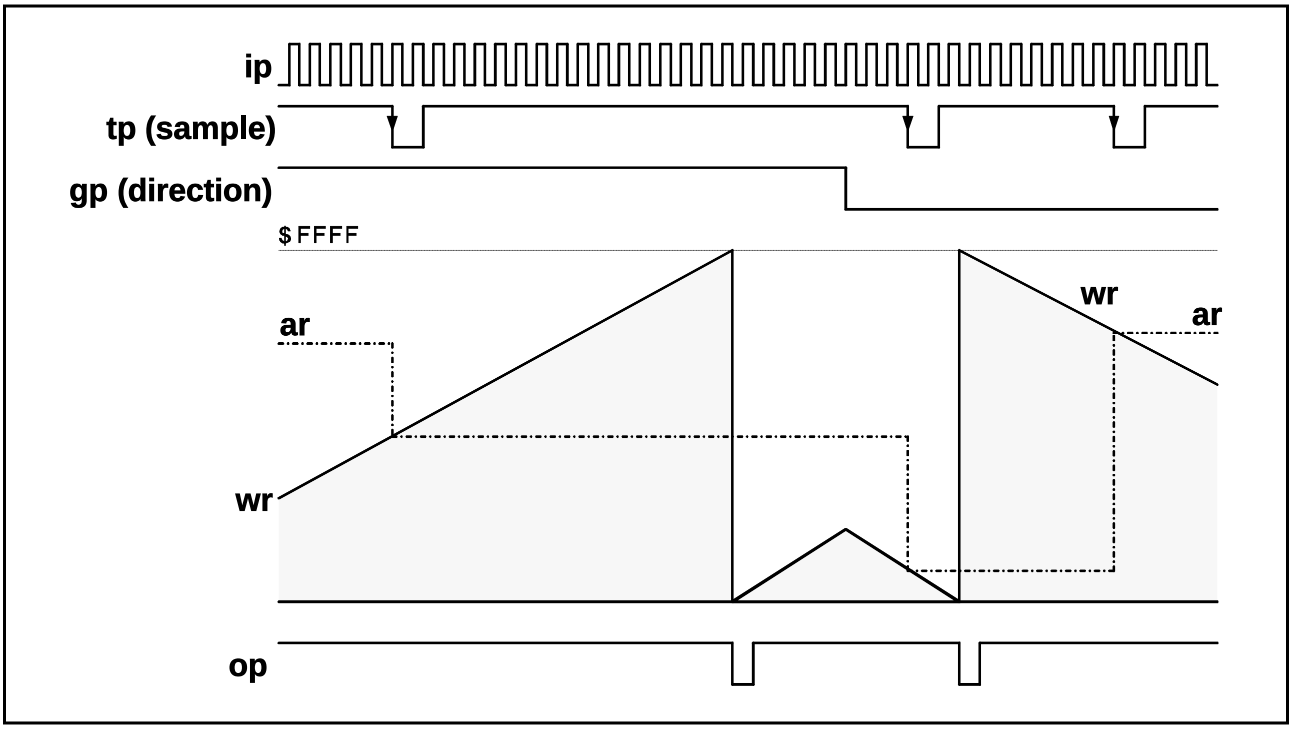
3*) As trigger pin 'real', 'hidden' or 'dummy pins' are possible:
tp = 1-16 or 17-32 (real)
tp = 33-40 or 41-48 (hidden)
tp = 49-56 or 57-64 (dummy)
tp = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

4*) As gate pins 'real' or 'hidden pins' are possible:
gp = 1-16 or 17-32 (real)
gp = 33-40 or 41-48 (hidden)
gp = 0 (no gate pin)

Otherwise the same conditions apply for gate pin and input pin.

STC* Value with which the auxiliary and the working register are preloaded after the procedure call.



Further parameters not shown:
`opol` = 0
`tedg` = 2

Fig. 4.3.6: Timing example for UDS operation

The cycle input (`ip`) counts the working register (`wr`) continually up or down (to max $FFFF). The counting direction is determined by following conditions:

`gp` (direction)	`opol`	counting direction
0	0	▼ down (decrement)
0	1	▲ up (increment)
1	0	▲ up (increment)
1	1	▼ down (decrement)

Table 4.3.5: Counting direction in UDS operation

With the active edge of the trigger pin (sample) the actual value of the working register (*wr*) is written into the auxilary register (*ar*).

The output pin (*op*) is set when the counter final value ($FFFF) is reached, independent from the counting direction.

Following circuit diagram gives an example on the daisy chaining of two UDS processes to a 32-bit counter.

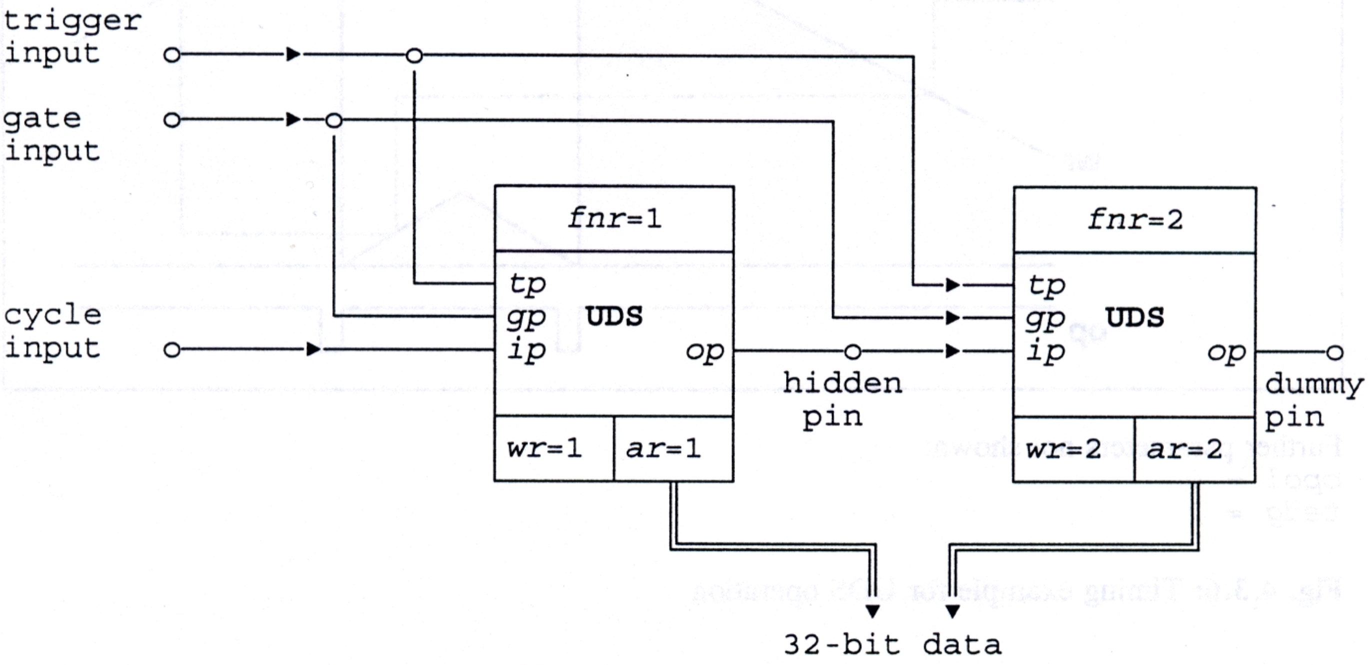


Fig. 4.3.7: Example for a 32-bit counter

4.3.10 TPC - two phase up-down counter

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
TPC	1-16	1*)	0/1	2*)	3	3*)	3	0	7	1-32	1-48	0	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) As output pin only a 'dummy pin' is useful:
op = 49-56 oder 57-64 (dummy)

2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

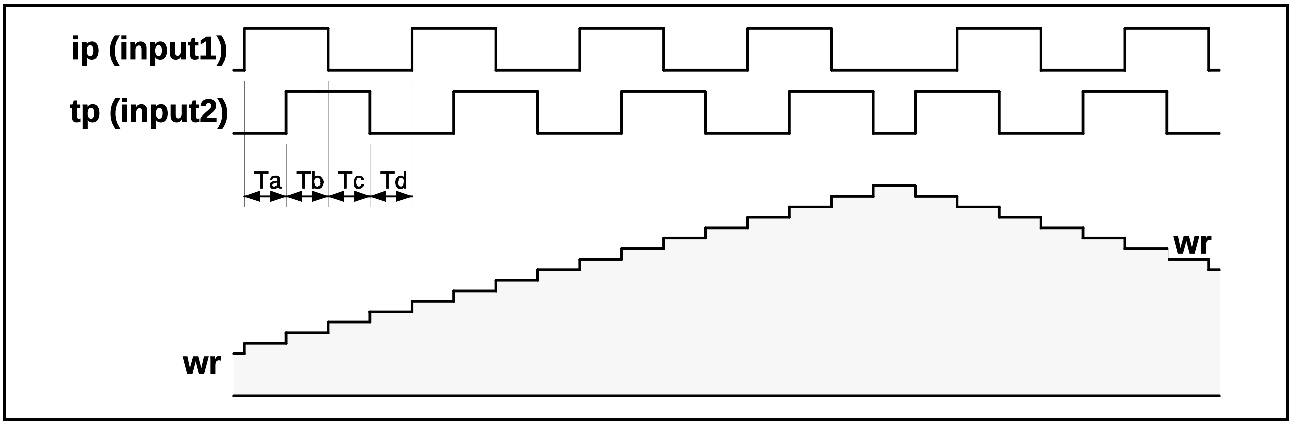
Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As trigger pin 'real' or 'hidden' pins are possible:
tp = 1-16 or 17-32 (real)
tp = 33-40 or 41-48 (hidden)
tp = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

STC* Value with which the working register is preloaded after procedure call.

The entry for the auxiliary register is not evaluated for this function, because the register is not required.



Ta,Tb,Tc,Td ≥ Pulse width resolution = 5μs

Further parameters not shown:
iedg = 3
tedg = 3

Fig. 4.3.8: Timing example for the operation

Depending on the phase position of the input pin (`ip`) to the trigger pin (`tp`) the working register (`wr`) is either counted up or down.

Input pin `ip`	Input pin `tp`	Counting direction
↑ 1 ↓ 0	0 ↑ 1 ↓	up (increase) (+1)
↑ 1 ↓ 0	1 ↓ 0 ↑	down (decrease) (-1)

Table 4.3.6: Counting direction in TPC operation

Pulse Processing Mode

4.3.11 FRS - free-running counter/timer with sampling

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
FRS	1-16	1*)	0/1	2*)	0-3	3*)	0-3	0	8	1-32	1-48	1-64	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) As ouput pins either 'real', 'hidden' or 'dummy' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)
op = 49-56 or 57-64 (dummy)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

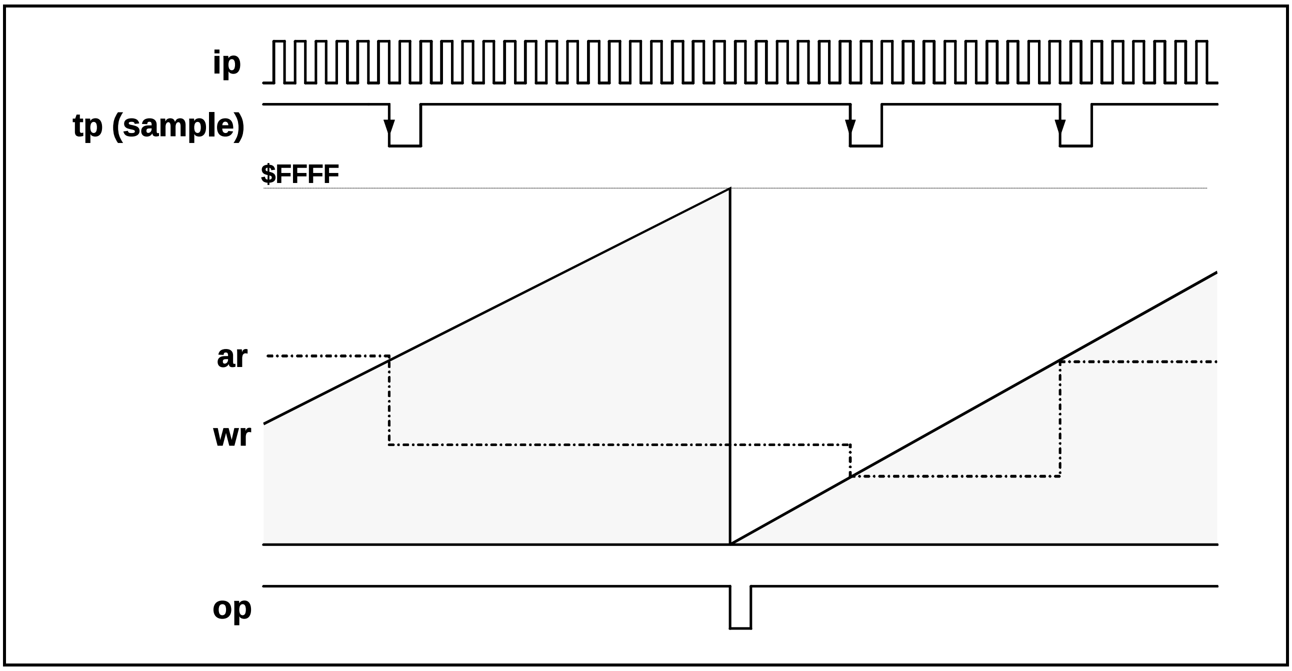
2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As trigger pin 'real' or 'hidden' pins are possible:
tp = 1-16 or 17-32 (real)
tp = 33-40 or 41-48 (hidden)
tp = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

STC* Value with which the auxiliary and working registers are preloaded after procedure call.



Further not shown pramaters:
`opol = 0`
`tedg = 2`
`gp   = 0`

Fig. 4.3.9: Timing examples for FRS operation

The register `wr` is counted up (with `mode = 8`) or down (with `mode = 108`) via the input cycle (`ip`).

The value of `wr` is taken over into the auxiliary register via the sample pulse (`tp`).

The output pin (`op`) is set at the overflow of register `wr`.

4.3.12 INS - interval counter/timer with sampling

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
INS	1-16	1*)	0/1	2*)	0-3	3*)	0-3	0	9	1-32	1-48	1-64	STC*

Parameters `fnr`, `wr`, `ar`, and `prld` will be explained in detail following the description of the parameter `mode`.

1*) As ouput pins either 'real', 'hidden' or 'dummy' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)
op = 49-56 or 57-64 (dummy)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

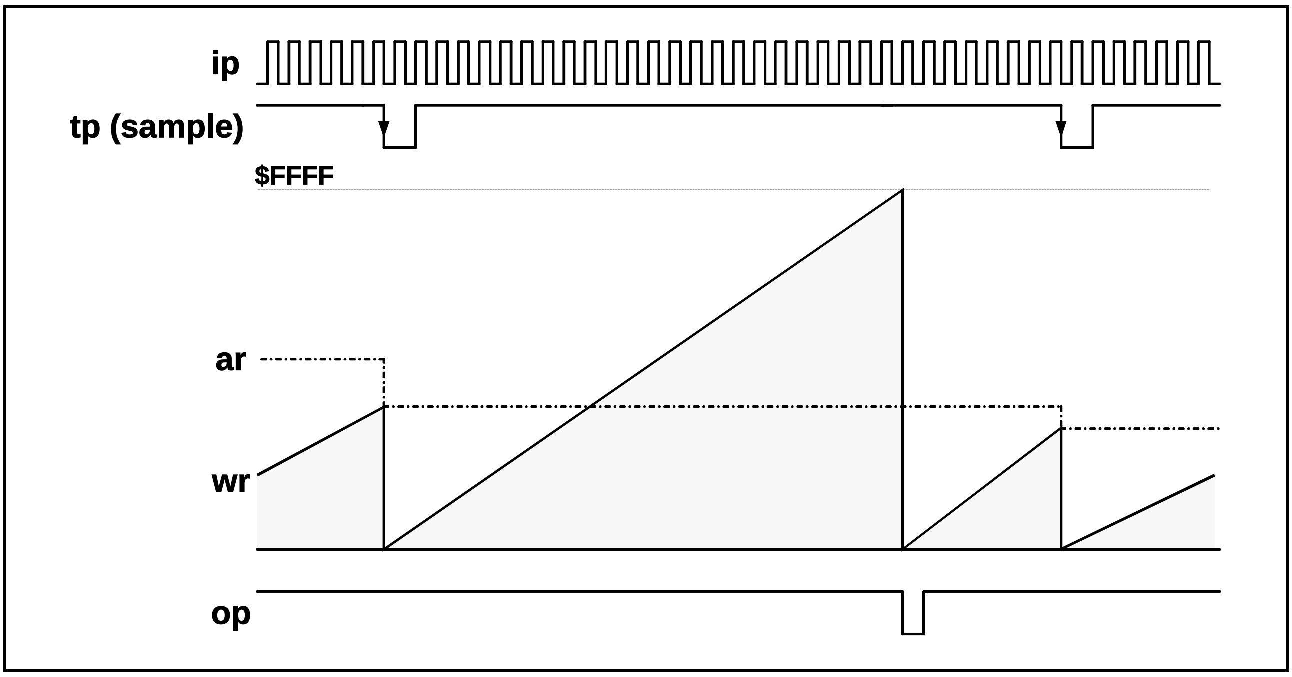
2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As trigger pin 'real' or 'hidden' pins are possible:
tp = 1-16 or 17-32 (real)
tp = 33-40 or 41-48 (hidden)
tp = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

STC* Value with which the auxiliary and working registers are preloaded after procedure call.



Further parameters not shown:
`opol = 0`
`tedg = 2`
`gp   = 0`

Fig. 4.3.10: Timing example for INS operation

The register *wr* is either counted up (with *mode* = 9) or down (with *mode* = 109) via the input cycle (*ip*).

The value of *wr* is taken over into the auxiliary register by means of the sample pulse (*tp*) and the register *wr* is reset.

The output pin (*op*) is set when the register *wr* overflows.

Pulse Processing Mode

4.3.13 FRC - free running counter/timer with compare

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
FRC	1-16	1*)	0/1	2*)	0-3	0	0	0	10	1-32	1-48	1-64	STC*

Parameters *`fnr`*, *`wr`*, *`ar`*, and *`prld`* will be explained in detail following the description of the parameter **`mode`**.

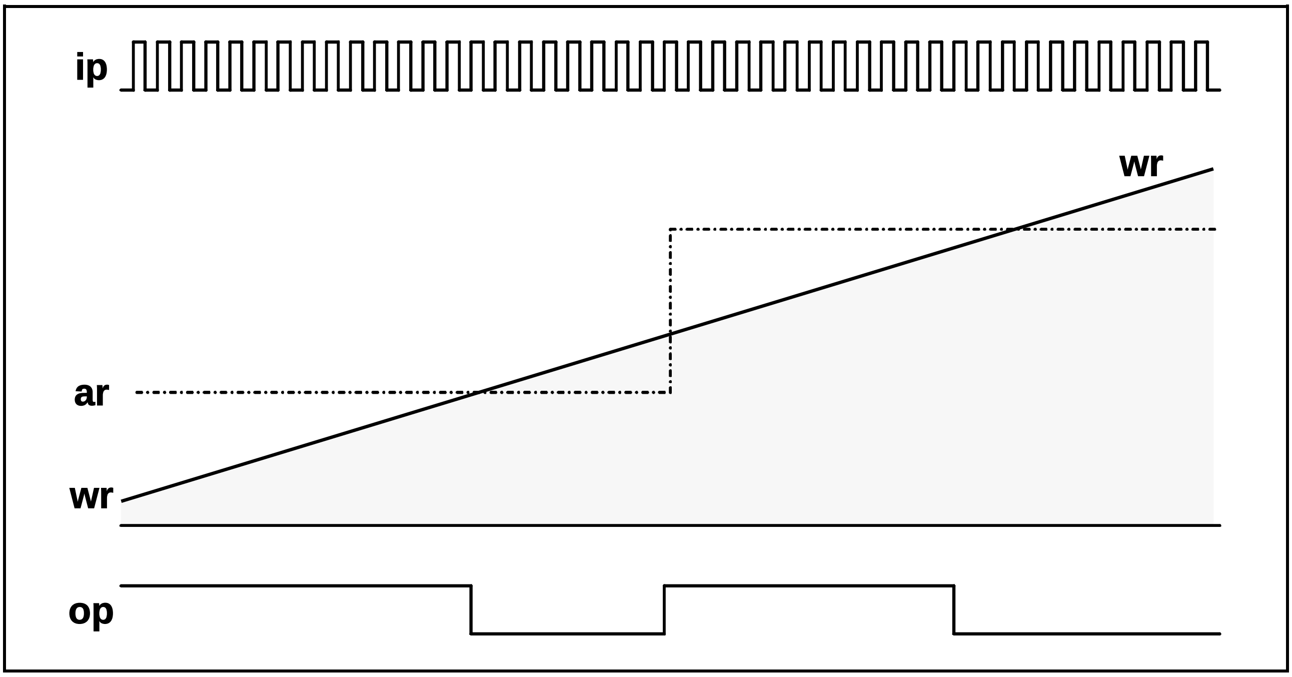
1*) As ouput pins either 'real' or 'hidden' pins are useful:
`op` = 1-16 or 17-32 (real)
`op` = 33-40 or 41-48 (hidden)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
`ip` = 1-16 or 17-32 (real)
`ip` = 33-40 or 41-48 (hidden)
`ip` = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

`STC*` Value with which the auxiliary and the working register are preloaded after the procedure call.



Further parameters not shown:
opol = 0
tp = 0
gp = 0

Fig. 4.3.11: Timing example for FRC operation

The register *wr* is counted up (with **mode** = 10) or down (with **mode** = 110) via the input cycle (*ip*).

The output pin (*op*) is activated, if the set status applies:

op := *wr* ≥ *ar*

4.3.14 OSC - one shot counter/timer with compare

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
OSC	1-16	1*)	0/1	2*)	0-3	3*)	0-3	0	11	1-32	1-48	1-64	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) As ouput pins either 'real' or 'hidden' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

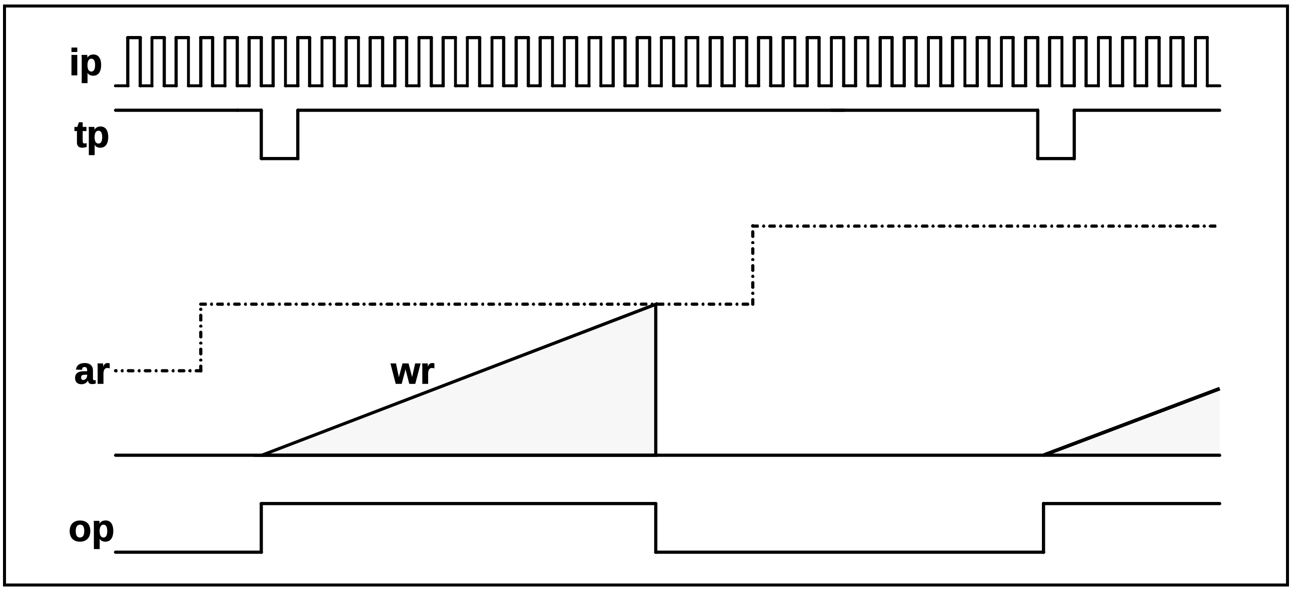
2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As trigger pin 'real' or 'hidden' pins are possible:
tp = 1-16 or 17-32 (real)
tp = 33-40 or 41-48 (hidden)
tp = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

STC* Value with which the auxiliary and working registers are preloaded after procedure call.



Further parameters not shown:
`opol = 0`
`tedg = 2`
`gp   = 0`

Fig. 4.3.12: Timing example for OSC operation

Following the active edge of trigger input *tp* the register *wr* is counted up (with *mode* = 10) or down (with *mode* = 111) via the input cycle (*ip*).

If the value of the register *wr* reaches the value of the register *ar*, register *wr* is reset and the output signal (*op*) is inverted. This status is retained until the next trigger pulse is received. After the reception of the trigger the output is again inverted and the counting process is started again.

4.3.15 GTC - gated counter/timer with compare

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
GTC	1-16	1*)	0/1	2*)	0-3	0	0	3*)	12	1-32	1-48	1-64	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) As ouput pins either 'real', 'hidden' or 'dummy' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)
op = 49-56 or 57-64 (dummy)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

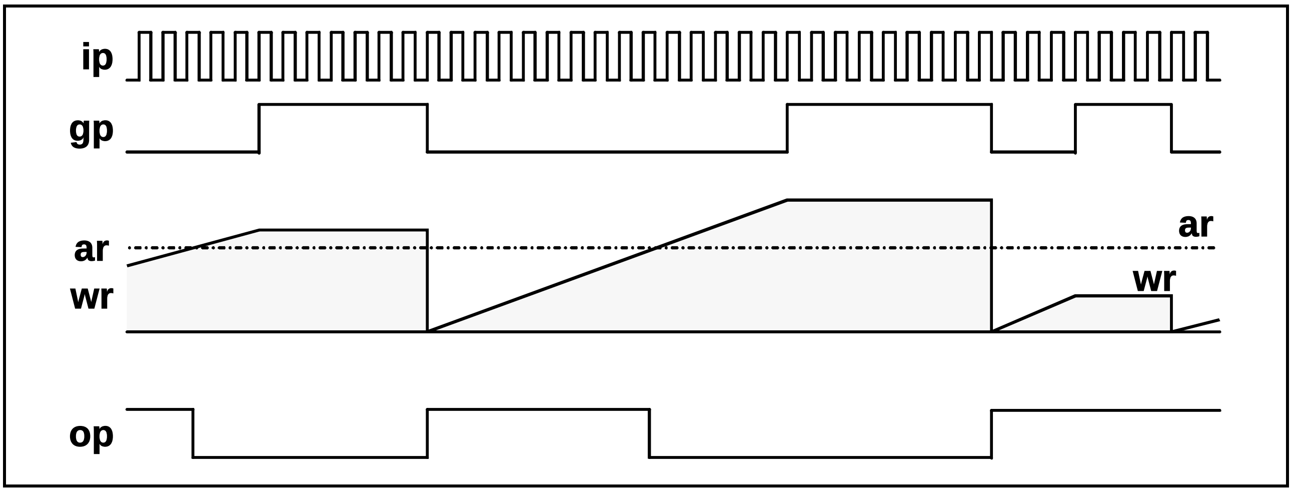
2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As gate pins 'real' or 'hidden' pins are possible:
gp = 1-16 or 17-32 (real)
gp = 33-40 or 41-48 (hidden)
gp = 0 (no gate pin)

Otherwise the same conditions apply for gate and input pin.

STC* Value with which the auxiliary and working registers are preloaded after procedure call.



Further parameters not shown:
`opol = 0`
`tp   = 0`

Fig. 4.3.13: Timing example for GTC operation

Following the falling edge of the gate signal (*gp)* the register *wr* is reset and counted up (with *mode* = 12) or down (with *mode* = 112) via the input cycle (*ip*). The falling edge stops the counting process.

If the value of the register *wr* reaches the value of the register *ar*, the output signal (*op*) is activated.

4.3.16 CTO - combination trigger one shot counter/timer

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
CTO	1-16	1*)	0/1	2*)	0-3	3*)	0-3	4*)	13	1-32	1-48	1-64	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) As ouput pins either 'real' or 'hidden' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

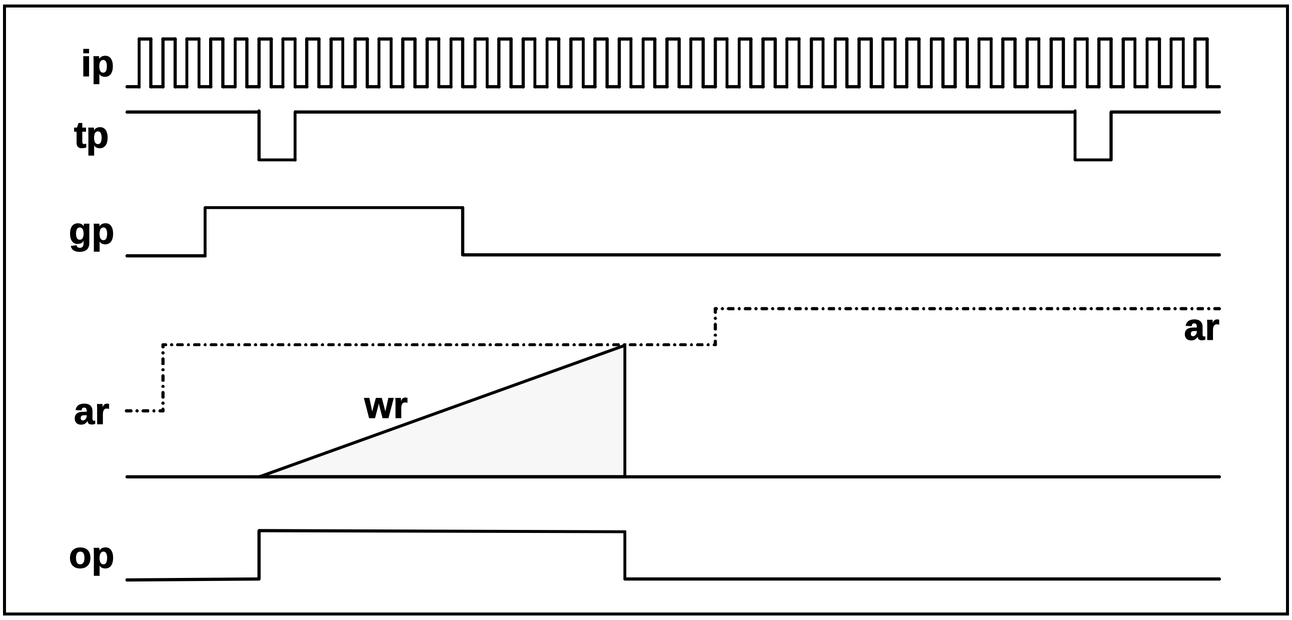
3*) As trigger pin 'real' or 'hidden' pins are possible:
tp = 1-16 or 17-32 (real)
tp = 33-40 or 41-48 (hidden)
tp = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

4*) As gate pins either 'real' or 'hidden' pins are useful:
gp = 1-16 oder 17-32 (real)
gp = 33-40 oder 41-48 (hidden)
gp = 0 (no gate pin)

Otherwise the same conditions apply for gate and input pins.

`STC*` Value with which the auxiliary and working registers are preloaded after procedure call.



Further parameters not shown:
opol = 0
tedg = 2

Fig. 4.3.14: Timing example for CTO operation

If the gate input (*gp)*, which here serves as trigger-enable signal, is set to '1', and if then a trigger signal (*tp)* is received, the register is counted up (with *mode* = 13) or down (with *mode* = 113) via the input cycle (*ip*).

Furthermore, by means of the active edge of the trigger signal the output (*op*) is inverted.

If the value of the register *wr* reaches the value of the register *ar*, the register *wr* is reset and the output signal (*op*) is inverted again. The register content remains reset and the actual output level is retained until the next trigger status is achieved.

Pulse Processing Mode

4.3.17 SIT - shift input

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
SIT	1-16	1*)	0/1	2*)	0-3	3*)	0-3	1*)	14	1-32	1-48	1-64	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) **In this function the same number has to be specified for the output pin and for the gate pin!** This function uses the output pin as input. If real pins are to be used, also a physical input has to be designed, here!

For the gate pin and the output pin either 'real' or 'hidden' pins are useful:
op = *gp* = 1-16 or 17-32 (real)
op = *gp* = 33-40 or 41-48 (hidden)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

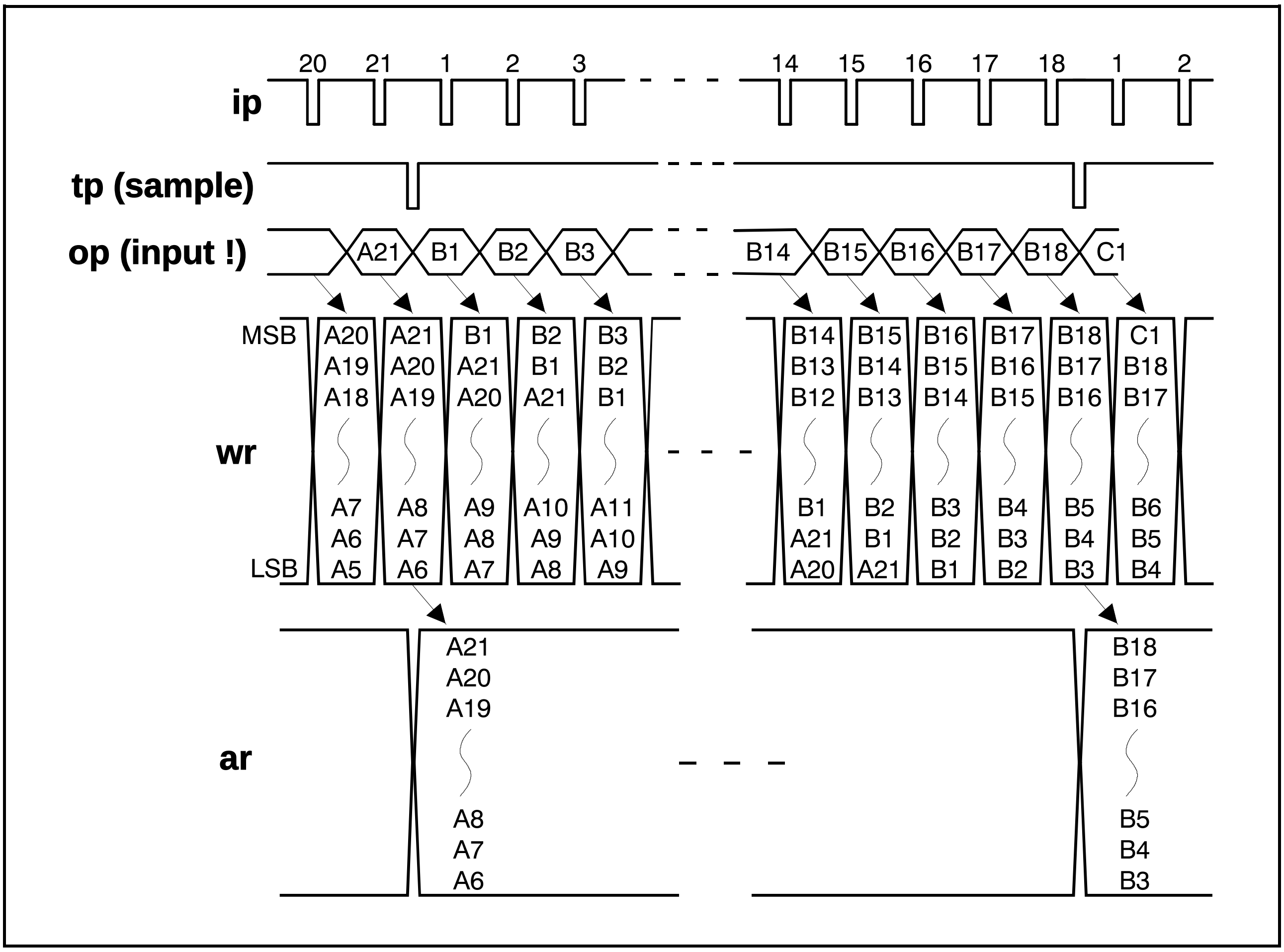
2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As trigger pins 'real', 'hidden' or 'dummy' pins are possible:
tp = 1-16 or 17-32 (real)
tp = 33-40 or 41-48 (hidden)
tp = 49-56 or 57-64 (dummy)
tp = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

STC* Value with which the auxiliary and working registers are preloaded after procedure call.



Further parameters not shown:
`opol` = 0
`tedg` = 2

Fig. 4.3.15: Timing example for SIT operation

By means of the input cycle `ip` the current level at pin `op` is taken over into the MSB of the working register (`wr`) and all other bits are shifted towards LSB.

By means of activating the sample signal (`tp`) the current value of the working register is taken over into the auxiliary register.

Note:
When implementing this function *HITACHI* did not choose the free register of the gate pin to select the signal to be read-in, but the register which is designed as output pin in the other functions (see also notes mentioned above on the selection of the output pin)!

Pulse Processing Mode

4.3.18 SOT - shift output

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
SOT	1-16	1*)	0/1	2*)	0-3	3*)	0-3	0	15	1-32	1-48	1-64	STC*

Parameters *fnr*, *wr*, *ar*, and *prld* will be explained in detail following the description of the parameter *mode*.

1*) As ouput pins either 'real', 'hidden' or 'dummy' pins are useful:
op = 1-16 or 17-32 (real)
op = 33-40 or 41-48 (hidden)
op = 49-56 or 57-64 (dummy)

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

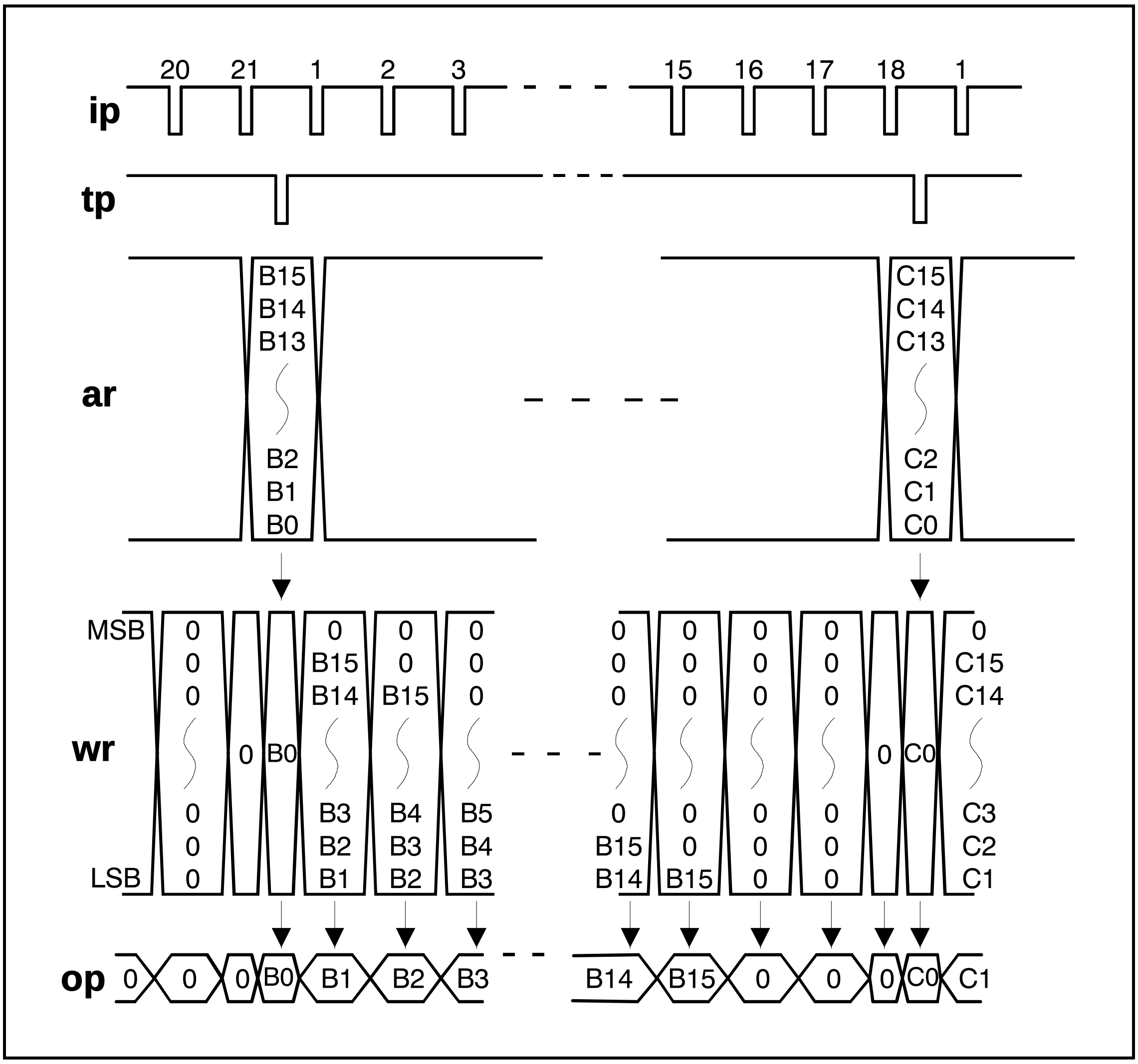
2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:
ip = 1-16 or 17-32 (real)
ip = 33-40 or 41-48 (hidden)
ip = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As trigger pins 'real' or 'hidden' pins are possible:
tp = 1-16 or 17-32 (real)
tp = 33-40 or 41-48 (hidden)
tp = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

STC* Value with which the auxiliary and working registers are preloaded after procedure call.



Further parameters not shown:
opol = 0
tedg = 2
gp = 0

Fig. 4.3.16: Timing example for SOT operation

By means of the active edge of the trigger pin (`tp`) the value of the auxiliary register `ar` is taken over into the working register (`wr`).

Via the input cycle `ip` the output pin `op` is set to value of the LSB of the `wr`. The bits are shifted towards LSB and the MSB is assigned with '0'. By doing so all bits of the working register are 'moved out' and the free elements are assigned with '0'.

The determination of the shift direction will be explained in the following command (SPO).

Pulse Processing Mode

4.3.19 SPO - shift parallel output

mode	*crd*	*op*	*opol*	*ip*	*iedg*	*tp*	*tedg*	*gp*	*mode*	*fnr*	*wr*	*ar*	*prld*
SPO	1-16	1*)	0/1	2*)	0-3	3*)	0-3	0	16	1-32	1-48	1-64	STC*

Parameters `fnr`, `wr`, `ar`, and `prld` will be explained in detail following the description of the parameter `mode`.

4.3.201*) In this function the output pins on which the bits of the shift register (`wr`) are to be put out are selected via the parameter `op.` The coding of the `op` becomes clear when the parameter is regarded as five-digit binary number. The transition still occurs as FIXED variable. The following table shows the bit-to-pin-assignment. The bits `O0` to `O4` are assigned to the bits of the parameter `op` as follows:

Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
O4	O3	O2	O1	O0

	`O4` = 1				`O4` = 0			
	shift-register bit		output pin HD1	output pin (HD2)	shift-register bit		output pin HD1	output pin (HD2)
`O0` = 1	0	►	1	(17)	0	►	33	(41)
	1	►	2	(18)	1	►	34	(42)
`O1` = 1	2	►	3	(19)	2	►	35	(43)
	3	►	4	(20)	3	►	36	(44)
`O2` = 1	4	►	5	(21)	4	►	37	(45)
	5	►	6	(22)	5	►	38	(46)
`O3` = 1	6	►	7	(23)	6	►	39	(47)
	7	►	8	(24)	7	►	40	(48)

Table 4.3.7: Output pins in SPO mode

Via `O4`=1 real pins are selected as output and via `O4`=0 hidden pins are selected. The real pins 9 to 16 (or 25 to 32) cannot be selected!
If the bits `O0...O3` are set to '0', the bits of the shift register are not output.

Example: Via `op` = 17 the shift-register bits 0 to 5 are output on the output pins 1 to 6.

It has to be taken care of that the pin direction of the real pins, as selected in the software, corresponds to the connected signals!

2*) 'Real pins', 'hidden pins' or the internal cycle can be used as input pins:

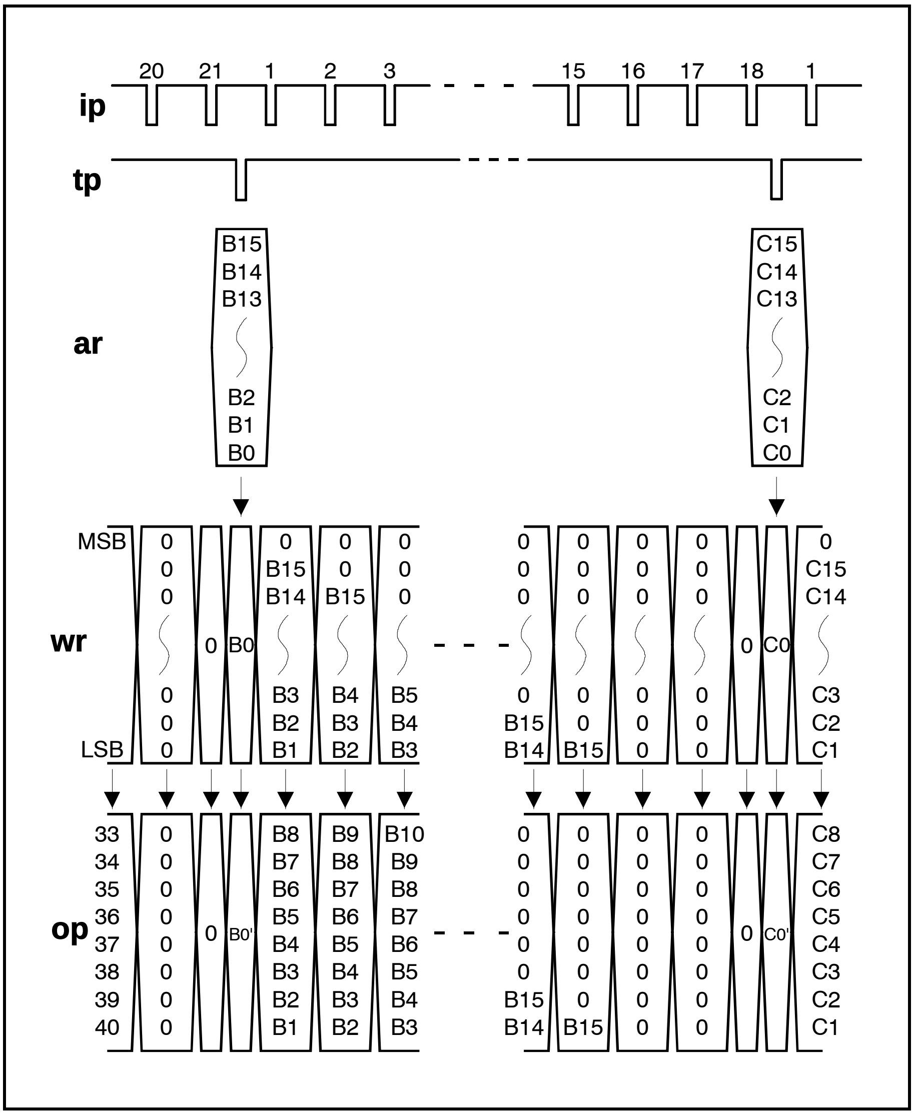
`ip` = 1-16 or 17-32 (real)
`ip` = 33-40 or 41-48 (hidden)
`ip` = 0 (internal cycle)

Pins 9...16 or 25...32 are wired as outputs at P2. They can still be used as input pins, if they are set by another process. **No external input signal can be applied to P2 for these pins!**
The I/O circuit of pins 1...8 or 17...24 can be programmed in groups of four either as output circuit or input circuit.

3*) As trigger pins either 'real', 'hidden' or 'dummy' pins are possible:
`tp` = 1-16 or 17-32 (real)
`tp` = 33-40 or 41-48 (hidden)
`tp` = 49-56 or 57-64 (dummy)
`tp` = 0 (no trigger)

Otherwise the same conditions apply for trigger and input pin.

`STC*` Value with which the auxiliary and working registers are preloaded after procedure call.



Further parameters not shown:
`opol` = 0
`tedg` = 1

Fig. 4.3.17: Timing example for SPO operation

The content of the auxiliary register (`ar`) is taken over into the working register `wr` via the active edge of the trigger signal.

Via the first following active edge of the input cycle `ip` the 8 LSB of the `wr` are put onto the chosen output pins. The cycle `ip` now shifts the bits towards the output with the highest number. By doing this the 8 MSB also reach the output pins.

The shift direction of functions SPO and SOT is preassigned via the three bits 'S0', 'S1' and 'S2'. In this implementation 'S1' is fixed to '0' and cannot be changed.

'S0' is set via the parameter opol:
opol = 0 → S0 = 0
opol = 1 → S0 = 1

'S2' is changed by adding the decimal value '100' to the *mode* parameter:

mode = 15 (SOT),	or *mode* = 16 (SPO)	sets S2 = 0
mode = 115 (SOT),	or *mode* = 116 (SPO)	sets S2 = 1

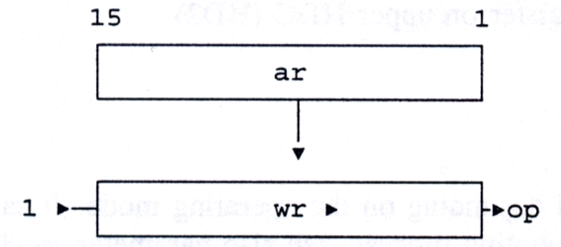
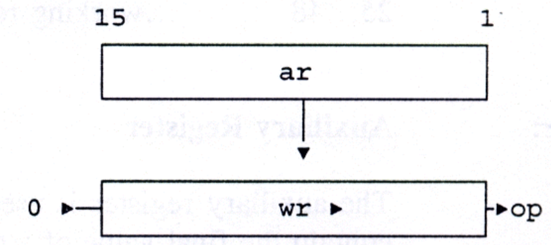
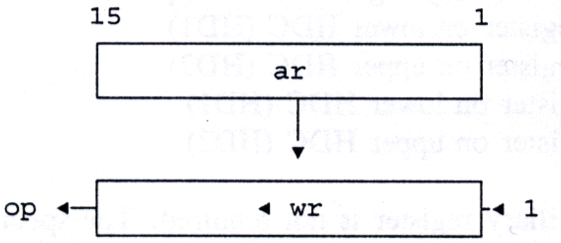
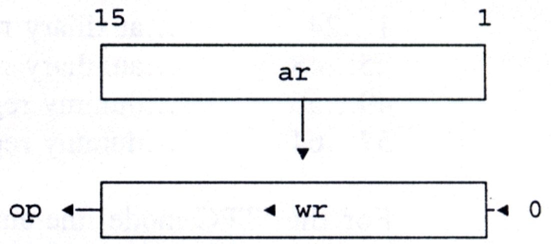
S2	S1	S0 (*opol*)	
		1	0
0	0		
1 (mode + 100)	0		

Table 4.3.8: Determination of the shift direction via *opol* and *mode*

`fnr` : Function_No.

The Function_No. specifies the process-table position at which the defined process is to be stored.

0	...no process
1...16	...process on lower HDC (HD1)
17...32	...process on upper HDC (HD2)

`wr`: Working Register

The working register is used depending on the operating mode. It can for instance be incremented or decremented for counting processes (see also parameter `mode`).

1...24	...working register on lower HDC (HD1)
25...48	...working register on upper HDC (HD2)

`ar`: Auxiliary Register

The auxiliary register is used depending on the operating mode. It can for instance contain the final value of a counting process (see also parameter `mode`).

0	...value of the auxiliary register is not required
1...24	...auxiliary register on lower HDC (HD1)
25...48	...auxiliary register on upper HDC (HD2)
49...56	...dummy register on lower HDC (HD1)
57...64	...dummy register on upper HDC (HD2)

For the 'TPC mode' the auxiliary register is not required. The specified value for this parameter is not evaluated (`ar` can e.g. be assigned with '0').

`prld`: Preload Auxiliary and Working Register

Preloading the auxiliary and the working registers.

`prld` = $0000...$FFFF

Attention!
The Function_No. (`fnr`), the working register (`wr`), the auxiliary register (`ar`) and all included pins must be on the same HD63143 controller!

4.4 Setting the HITACHI-Pulse Register -SUPDPI

Declaration:

```
SPC SUPDP1 ENTRY (FIXED, FIXED, FIXED) GLOBAL;
```

Variable definition:

```
DCL (crd, reg_nr, value) FIXED;
```

Value range:

crd : board no.
0 ...ignore board
1...16 ...board 1 to 16

reg_no : register no. (see also *wr, ar*)
1...24 ...register of HD1 (channel 1 to 16)
25...48 ...register of HD2 (channel 17 to 32)

value : register value
value = 0...65535

Procedure call:

```
CALL SUPDP1 (crd, reg_nr, value)
```

4.5 Reading the HITACHI-Pulse-Registers -GUPDPI

Declaration:

```
SPC GUPDP1 ENTRY (FIXED, FIXED) RETURNS (FIXED) GLOBAL;
```

Variable definition:

```
DCL (crd, reg_nr, value) FIXED;
```

Value range:

crd : board no.
0 ...ignore board
1...16 ...board 1 to 16

reg_no : register no. (see also *wr, ar*)
1...24 ...register of HD1 (channel 1 to 16)
25...48 ...register of HD2 (channel 17 to 32)

value : register value
value = 0...65535

Procedure call:

```
value = GUPDP1 (crd, reg_nr)
```