Application Note to CAN/402-Boards
Potential Interoperability Problems with Windows® or Linux® OS

This document is to alert users to potential interoperability problems that affect esd CAN/402 boards which are equipped with the Pericom® PCI-to-PCI bridge PI7C9X111SL.

Depending on the host computer system the following esd CAN/402 articles may be affected:

CAN-PCI/402:

Article	Order No.
CAN-PCI/402-1	C.2049.02
CAN-PCI/402-1-D	C.2049.03
CAN-PCI/402-2	C.2049.04
CAN-PCI/402-2-D	C.2049.05
CAN-PCI/402-4/2Slot	C.2049.06
CAN-PCI/402-4/2Slot-D	C.2049.07
CAN-PCI/402-B4/1 Slot	C.2049.08
CAN-PCI/402-1-LP	C.2049.32
CAN-PCI/402-1-LP-2	C.2049.34
CAN-PCI/402-2-FD	C.2049.64

PMC-CAN/402:

Article	Order No.
PMC-CAN/402-4-FD	C.2028.68
PMC-CAN/402-4-FD-IRIG-B	C.2028.69
PMC-CAN/402-4-FD-T	C.2028.78

CPCI-CAN/402:

Article	Order No.
CPCI-CAN/402-4	I.2332.08
CPCI-CAN/402-4-FD	I.2332.68
CPCI-CAN/402-4-FD-T	I.2332.76
CPCI-CAN/402-4-FD-R	I.2332.78

Windows Operating System:
Potential Interoperability Problem with enabled PCI Express Native Control Mode

Problem Description

Microsoft Windows operating systems including Windows® Vista, Windows Server 2008, and later versions include a feature called "PCI Express Native Control". Many current motherboards offer support for the PCI Express Native Control feature in their BIOS.

If this feature is enabled by Windows, it enforces additional mandatory features which are not implemented in the bridge of the CAN-PCI/402 / PMC-CAN/402 / CPCI-CAN/402 boards. This may prevent the start of the default PCI-to-PCI bridge driver (Code 10). This problem occurs for example on most ACER PC Windows systems .

Based on our information Pericom does not plan to revise the silicon of the PCI-to-PCI bridge to be compatible with the Windows supplied bridge driver.
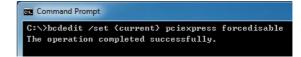
Solution: Disabling PCI Express Native Control Feature in Windows

The PCI Express Native Control can be switched off by commands in the command prompt window with administrator rights.

Use the command `BCDEdit /set`

to set a boot entry option value in the Windows boot configuration data store (BCD):

1. Boot the Windows system.

2. Open the command prompt window with administrator rights (right-click to `C:\Windows\System32\cmd.exe` and select "Run as Administrator").

3. Enter the command
   `bcdedit /set {current} pciexpress forcedisable`


```
C:\>bcdedit /set {current} pciexpress forcedisable
The operation completed successfully.
```

4. Restart your computer.

Note:

If you disable the PCI Express Native mode this may cause loss of other system features, such as Hot Plug, which requires the PCI Express Native mode (see link to MSDN for more details).
To restore the previous state type the following commands:

```
bcdedit /deletevalue {current} pciexpress
 or
bcdedit /set {current} pciexpress default
```

Links to further Information

- About `BCDEdit /set` command: https://learn.microsoft.com/en-us/windows-hardware/drivers/devtest/bcdedit--set
- About PCI Express Native Control: https://learn.microsoft.com/en-us/previous-versions/windows/hardware/design/dn631753(v=vs.85)
- PCI-SIG website: https://pcisig.com/

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Linux Operating System:
Potential Interoperability Problem caused by Active State Power Management Reconfiguration

Problem Description

Recent Linux kernels try to reconfigure and optimize the Active State Power Management settings of PCI Express links. In the course of the reconfiguration the kernel triggers an erratum of the PCI-to-PCIe reverse bridge PI7C9X111SL that is used on the shown products. Caused by this erratum the PCIe link stays in the link retraining state and is not usable.

This can be diagnosed by looking at the lspci output for the PCIe device behind the Pericom bridge that looks like this in the failure case:

```
root@host# lspci -s 3:0.0 -v -x
03:00.0 CANBUS: ESD Electronic System Design GmbH Device 0402 (rev ff) (prog-if ff)
        !!! Unknown header type 7f
00: ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
10: ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
20: ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
30: ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff ff
```

Solutions: Booting the System with the additional Kernel Parameter "pcie_aspm=off"

As a workaround you may boot the system with the additional kernel parameter "pcie_aspm=off" which will disable ASPM reconfiguration for the whole machine.

If you are able to build your Linux kernel yourself you may apply this patch to introduce a workaround for this Pericom reverse bridge.

```
--- drivers/pci/pcie/aspm-orig.c        2018-04-01 23:20:27.000000000 +0200
+++ drivers/pci/pcie/aspm.c     2018-11-07 14:08:58.301927694 +0100
@@ -218,6 +218,7 @@
        child = list_entry(linkbus->devices.next, struct pci_dev, bus_list);
        BUG_ON(!pci_is_pcie(child));

+
        /* Check downstream component if bit Slot Clock Configuration is 1 */
        pcie_capability_read_word(child, PCI_EXP_LNKSTA, &reg16);
        if (!(reg16 & PCI_EXP_LNKSTA_SLC))
@@ -251,6 +252,16 @@
        /* Retrain link */
        reg16 |= PCI_EXP_LNKCTL_RL;
        pcie_capability_write_word(parent, PCI_EXP_LNKCTL, reg16);
+       if (0x12d8 == parent->vendor && 0xe111 == parent->device) {
+           /*
+            * Due to an erratum in the Pericom PI7C9X111SLB bridge in
+            * reverse mode the retrain link bit needs to be cleared
+            * manually to allow the link training to succeed.
+            */
+           pci_info(parent,"PI7C9X111SLB workaround: Clear PCI_EXP_LNKCTL_RL again.\n");
+           reg16 &= ~PCI_EXP_LNKCTL_RL;
+           pcie_capability_write_word(parent, PCI_EXP_LNKCTL, reg16);
+       }

        /* Wait for link training end. Break out after waiting for timeout */
        start_jiffies = jiffies;
```

An equivalent patch was submitted to the linux-pci kernel mailing list (see https://lore.kernel.org/linux-pci/20190406143031.GB200379@google.com/T/) but it will take some time until it will show up in the production kernels of Linux distributions.

The mentioned patch hit the Linux mainline kernel with version 5.2.0.
The patch also has been backported to the following mainline stable kernels:
    5.1.5
    5.0.19
    4.19.46
    4.9.179
    3.16.74

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All data are subject to change without prior notice.
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