

# XMC-CAN/402-FD-LINIO

XMC Board with 4x CAN FD, 2x LIN and 4 Digital Inputs/Outputs

## XMC Board with FPGA for 4 CAN FD, 2 LIN and 4 Digital IO Interfaces

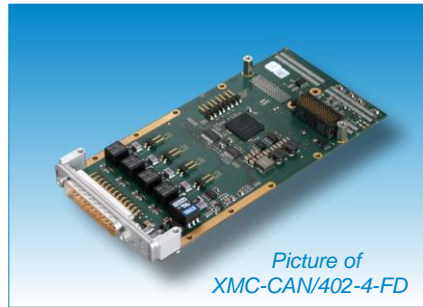
- 4 High-Speed CAN FD interfaces according to ISO 11898-2, up to 8 Mbit/s
- CAN termination electronically switchable
- Bus mastering and local data management by FPGA (esdACC)
- PCI bus according to PCI Local Bus Specification 3.0
- Supports MSI (Message Signalled Interrupts)
- 2 LIN interfaces
- 4 Digital Input/Output channels
- Optionally for extended temperature range
- DSUB25 connector in the front panel, an optional adapter to 5x DSUB9 is available

## Wide Range of Operating System Support and Advanced CAN Diagnostic

- Software drivers for Windows® and Linux® included free of charge
- Optional CAN/LIN layer 2 software drivers for real-time operating systems
- ISO 16845:2004 certified esd Advanced CAN Core (esdACC)
- High resolution hardware timestamps

## LIN Interfaces

- Physical layer of the LIN interfaces according to ISO 17987-4:2016
- Bit rate programmable up to 20 kbit/s
- Automatic bit rate detection and resynchronisation
- Commander and Responder work modes
- Switchable LIN Commander pull-up resistors



## CAN FD Interfaces

The XMC-CAN/402-FD-LINIO comes with four independent CAN FD interfaces according to ISO 11898-1, which are driven by the ISO 16845:2004 certified esdACC (esd advanced CAN Core) implemented in the FPGA. **All CAN FD interfaces are fully backwards compatible with CAN CC.**

## CAN Data Management

The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU load. Due to the usage of MSI (Message Signaled Interrupts) the XMC-CAN/402-FD-LINIO can be operated for example in Hypervisor environments. It provides high resolution hardware timestamps.

## LIN Interfaces

Two additional LIN interfaces are designed according to ISO 17987-4:2016. In addition to the CAN esdACC cores the FPGA carries two LIN IP cores for the control of the physical layers of the LIN interfaces

## Digital Input/Output

Four digital I/Os that can be set individually as input (interrupt capable) or output. The I/O-voltage can be switched between 3.3V or 5V by software. Input latency (signal to interrupt) 1µs, with a minimum pulse width of 2 µs.

## Optional Adapter Cable

Use the adapter to connect digital I/Os, CAN and LIN interfaces via 5 DSUB9 connectors.

## Rough Environment

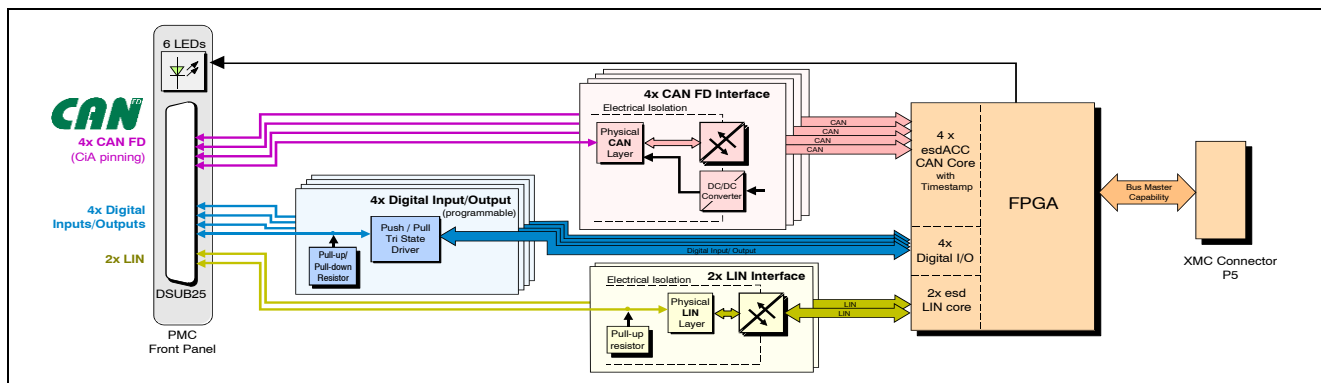
Optionally, the XMC-CAN/402-FD-LINIO-T version is available for usage in an extended temperature range.

## Software Support

Windows and Linux  
(NTCAN-API and NTLIN-API)

The CAN/LIN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Real-time OS (NTCAN-API and NTLIN-API)  
CAN/LIN layer 2 drivers e.g. for QNX® can be ordered separately, others on request. No additional driver is required to control the I/Os. This is done via the NTCAN-API (CAN events).



## Technical Specifications:

<b>XMC Interface:</b>	
PCIe® port	PCI Express Spec. 1.1, Link width 1x, PCI bus master capability
<b>Interfaces:</b>	
CAN	4x CAN FD (ISO 11898-2), galvanic isolation, bit rates from 10 kbit/s up to 8 Mbit/s esdACC in FPGA, acc. to ISO 11898-1
LIN	2x LIN according to ISO 17987-4:2016, up to 20 kbit/s
Digital IO	4 channels, each selectable as input or output; nom. IO-voltage: 3.3V or 5V, not galvanically isolated max. output current: @ 3.3V: 24 mA, @ 5V: 32 mA
<b>General:</b>	
Power supply	3.3 V I <sub>MAX</sub> < approx. 1.5 A, I <sub>TYP</sub> = 0.8 A
Ambient temp.	Standard range: 0 °C ... +80 °C (C.2018.70) Extended range: -40 °C ... +85 °C (C.2018.71)
Rel. humidity	Max. 90 % (non-condensing)
Dimension	149 mm x 74 mm x 10 mm
Connector	XMC: P5, (XMC connector acc. to VITA 42.3) CAN, LIN, IO: DSUB25 (4x CAN FD, 2x LIN, 4x Digital IO)

<b>Order Information:</b>		
<b>Hardware</b>		<b>Order No.</b>
XMC-CAN/402-FD-LINIO	PMC Board, 4x CAN FD, 2x LIN, 4x Digital IOs via DSUB25	C.2018.70
XMC-CAN/402-FD-LINIO-T	As C.2018.70 but for extended temperature range	C.2018.71
<b>Accessories</b>		
CAN Cable 1xDSUB25-to5xDSUB9_LINIO	Cable 1x DSUB25 to 5x DSUB9 for CAN and LIN and digital I/Os	C.2047.17
<b>Software Support <sup>1</sup></b>		
CAN layer 2 drivers for Windows/Linux are included in delivery free of charge. Additional CAN layer 2 object licences including CD-ROM:		
CAN-DRV-LCD QNX	Object Licence for QNX6, QNX7	C.1101.32
<sup>1</sup> For detailed information about driver availability for your operating system please contact our sales team.		
<b>Related Products</b>		
XMC-CAN/402-4-FD	XMC board, 4 CAN FD interfaces	C.2018.68
PMC-CAN/402-FD-LINIO	PMC version of the LINIO board	C.2028.70
PMC-CAN/402-FD-LINIO-T	As C.2028.70 but for ext. temp.	C.2028.71

# XMC-CAN/402-FD-LINIO

## Driven by esdACC-FD (Advanced CAN Core)



### Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Supported CAN FD bit rates: From 10 kbit/s up to 8 Mbit/s
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Disable Automatic Retransmission (DAR) (Single-shot transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Self-reception mode (reception of 'own' messages)
- Busload measurement



### Superior esdACC Features <sup>1</sup>:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case  $\leq 62.5$  ns, usually 12.5 ns)
  - Timestamping complies with the CiA 603 specification
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-real-time operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64-bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX

### Superior esdACC Features (continued) <sup>1</sup>:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx® Spartan® and Intel® Cyclone® FPGAs.

<sup>1</sup> Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.