PMC-CAN/400-4

4x CAN: Layer 2, CANopen®, J1939 or ARINC 825, optional IRIG-B

PMC Board with FPGA for 4x CAN via DSUB25

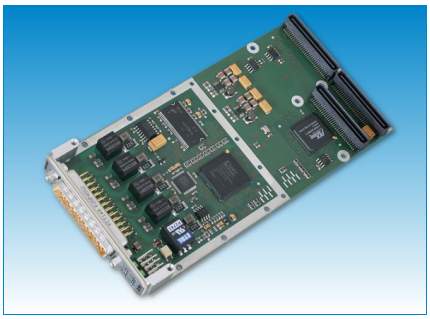
- 4 High-Speed CAN interfaces acc. to ISO 11898-2
- Bus mastering and local data management by FPGA (esdACC)
- PCI bus according to PCI Local Bus Specification 2.2
- All I/O-signals via 25-pin DSUB in the front panel

Wide Range of Operating System Support and advanced CAN Diagnostic

- ARINC 825, CANopen and J1939 protocol libraries are available
- esd Advanced CAN Core (esdACC) technology
- High resolution hardware timestamps
- Error simulation support

Variety of Hardware Designs

- IRIG-B input (option)
- Customized PMC-CAN/400-4 versions are available on request for extended temperature range or as conduction cooled version



CAN Data Management

The four independent CAN nets according to ISO 11898-1 are driven by the esd Advanced CAN Core (esdACC) CAN controller implemented in the Xilinx® Spartan® 3e FPGA.
Controlled by the FPGA the PMC-CAN/400-4 supports bus mastering as an initiator, meaning that it is capable of initiating write cycles to the host CPU's RAM independent of the CPU or the system DMA controller. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and reduced host CPU load.

The PMC-CAN/400-4 provides high resolution hardware timestamps.

IRIG-B

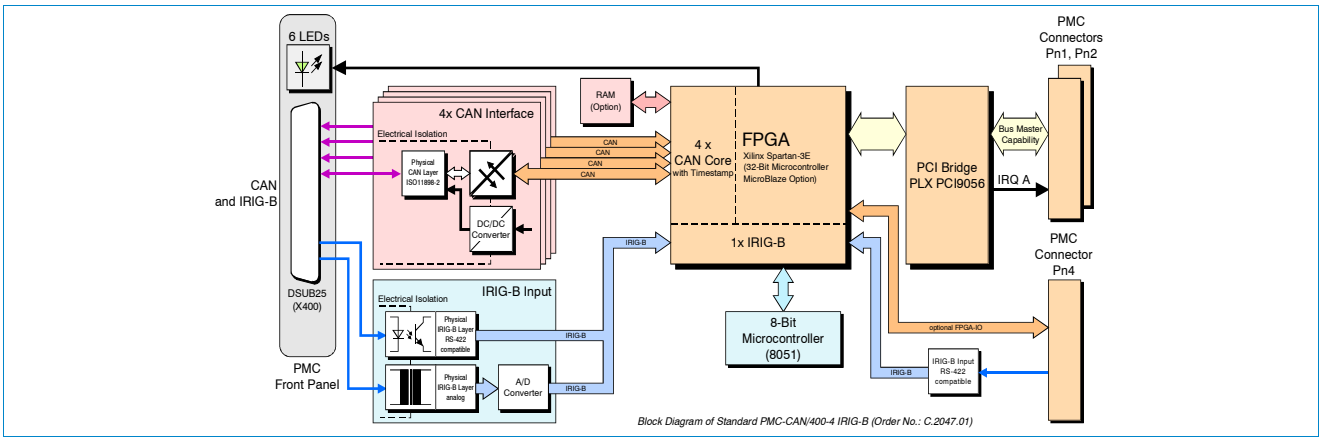
The optional IRIG-B interface offers inputs for analog or RS-422 IRIG-B coded signals. Both are electrically isolated.
IRIG-B evaluation is controlled by an additional microcontroller.

Software Support[1]

CAN layer 2 (NTCAN-API) software drivers are available for Windows®, Linux®,QNX®, VxWorks®, RTX and On Time RTOS-32.
Libraries for the higher layer protocols CANopen,J1939 and ARINC825 are available.
Additional free-of-charge esd CAN tools for Windows offer efficient setup and analysis of CAN applications and networks.

Customization on Request

As customized solutions an extended temperature range version and a conduction cooled version of the PMC-CAN/400-4 are available on request.
Additionally, esd offers a VMEbus carrier board in conduction cooled design to carry up to two conduction cooled PMC boards.



Block Diagram of Standard PMC-CAN/400-4 IRIG-B (Order No.: C.2047.01)

Technical Specifications:

PMC Interface and Microprocessor:	
PCI	PCI 2.2, 32 bit 33/66 MHz, 3.3 V (5 V tolerant, Universal board), PCI bus master capability
Memory	BlockRAM: 72 KB, DDR-SDRAM: 64 MB
Microprocessor	optional 32-bit µC in FPGA (MicroBlaze)
CAN:	
Interface	4x CAN high-speed interface according to ISO11898-2, differential,electrically isolated, bit rate up to 1 Mbit/s
CAN controller	esdACC in FPGA Spartan 3e, according to ISO 11898-1
IRIG-B Input Option:	
Interface	1x analog and 1x RS-422 compatible (both electr. isolated), 1x RS-422 compatible (at PN4 only)
Controller	8051 microcontroller
General:	
Ambient temperature	0 °C ... +50 °C Customized versions (on request only): Extended temperature range: -20...+75 °C Conduction cooled: -40...+85 °C
Rel. humidity	Max. 90 % (non-condensing)
Power supply	5 V and 3.3 V
Connectors	Pn1, Pn2, Pn4, DSUB25
LEDs	4x CAN status, 1x IRIG-B, 1x module status

Order Information:

Hardware	Order No.
PMC-CAN/400-4 4x CAN, 1x IRIG-B	C.2047.01
PMC-CAN/400-4 4x CAN	C.2047.03

CAN layer 2 drivers for Windows and Linux are included in delivery.

Accessories

CAN/400-4-1C5	Adapter cable DSUB25 to 5x DSUB9	C.2047.18
CAN/400-4-1C4	Adapter cable DSUB25 to 4x DSUB9	C.2047.19

Software Support

Additional CAN layer 2 object licences including CD-ROM[1]:	
CAN-DRV-LCD VxWorks	C.1101.55
CAN-DRV LCD QNX	C.1101.32
CAN-DRV-LCD RTX (incl. RTX64)	C.1101.35
CAN-DRV-LCD On Time RTOS-32	C.1101.45
Higher CAN layer protocols including CD-ROM[1]:	
CANopen-LCD Windows/Linux, VxWorks, QNX or RTX	C.1101.xx
J1939 Stack for Windows, Linux or RTX	C.1130.xx
ARINC825-LCD Windows/Linux, VxWorks, QNX, RTX	C.1140.xx

1 For detailed information about driver availability for your operating system please contact our sales team.

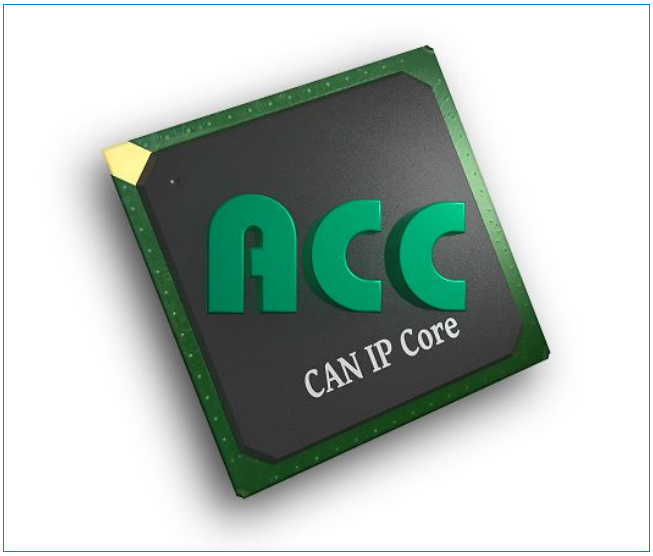
esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany
Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu

PMC-CAN/400-4

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Bit rates from 10 kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)



Superior esdACC Features [1]:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64 bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:

- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-bit microcontroller to further relieve host CPU
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.

[1] Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.

esd electronic system design gmbh
Vahrenwalder Str. 207
30165 Hannover / Germany

Phone: +49 (0) 511 3 72 98-0
Fax: +49 (0) 511 3 72 98-68
E-mail: info@esd.eu