



CPCISerial-CAN/402-2-FD

CompactPCI® Serial (PCIe®) Board with 2 CAN FD Interfaces

CompactPCI Serial Board with Altera® FPGA for 2x CAN FD via DSUB9 Connectors

- High-speed CAN FD interfaces acc. to ISO 11898-2, bit rate up to 5 Mbit/s
- Bus mastering and local data management by FPGA (esdACC)
- PICMG® CPCI-S.0 standard supporting high-speed PCI Express® interface lines
- Selectable CAN termination on board and cut-out in the front panel for jumper view
- Supports MSI (Message Signaled Interrupts)

Wide Range of OS Support and Advanced CAN Diagnostic

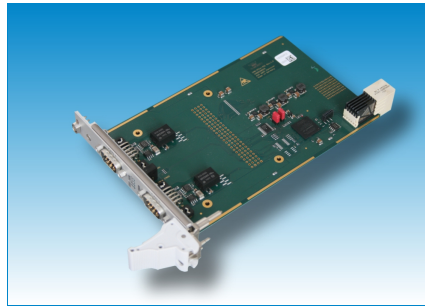
- Software drivers for Windows® and Linux® included free of charge
- Optional CAN layer 2 software drivers for real-time operating systems
- CANopen®, J1939 and ARINC 825 protocol libraries
- ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology
- High resolution hardware timestamps

Advanced CAN Controller

- esdACC technology offers highest CAN performance and diagnostic

Customization on Request

- Ext. temperature range: -40° C ... +75° C
- Error simulation support
- All signals via Rear I/O (P3)



CAN FD

The CPCISerial-CAN/402-2-FD is a CompactPCI Serial board with two electrically isolated CAN FD interfaces, according to ISO 11898-1:2015. The CAN FD interfaces are driven by the ISO 16845:2004 certified esdACC (esd advanced CAN Core) implemented in the Altera FPGA. With a higher bit rate in the data phase in combination with the increase of efficiency by a higher number of user-data bytes, CAN FD offers a higher data throughput while maintaining the benefits of Classical CAN. The CPCISerial-CAN/402-2-FD is fully backwards compatible with CAN and can be also used in Classical CAN applications.

CAN Data Management

The FPGA supports bus mastering (firstparty DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and a reduced host CPU

load.

Due to the usage of MSI the CPCISerial-CAN/402-2-FD can be operated for example in Hypervisor environments. The CPCISerial-CAN/402-2-FD provides high resolution 64-bit hardware timestamps for CAN messages.

Software Support

Windows and Linux (NTCAN-API)

The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Realtime OS (NTCAN-API)

CAN layer 2 drivers for e.g. QNX®, RTX64® and VxWorks® can be ordered separately.

Higher Layer Protocols

(Classical CAN application only)

Higher Layer Protocols are available for many operating systems (see order info):

- CANopen Master- and Slave-Stack
- J1939
- ARINC825

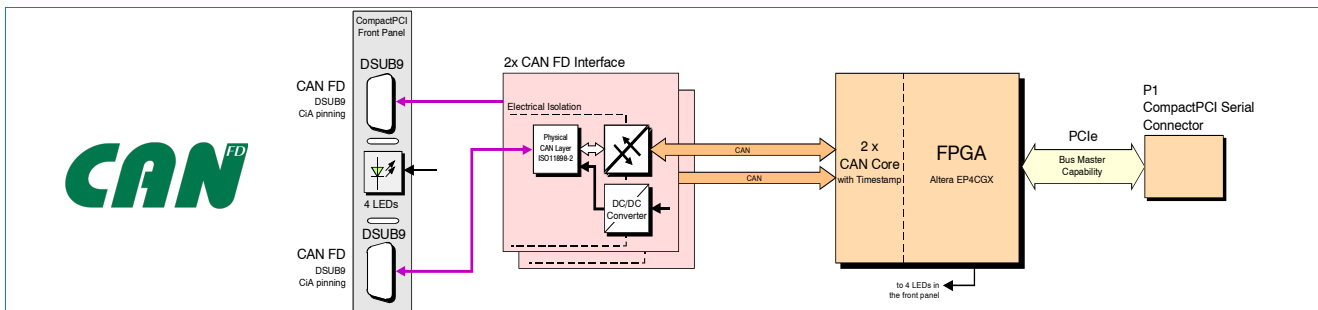
Additional free-of-charge esd CAN tools for Windows are downloadable from our website. The tools offer efficient setup and analysis of CAN applications and networks.

Customization on Request

Customized options are available for customized series production in reasonable quantities. Please contact our sales team for detailed information.

Related Products

The CPCISerial-CAN/402-4-FD provides 4 CAN FD interfaces via a DSUB25 connector.



Technical Specifications:

CompactPCI Serial Interface:	
Interface	PICMG CPCI-S.0 Rev. 1.0, PCI Express Rev. 1.0a, Link width 1x
CAN:	
Interface	2x CAN FD acc. to ISO11898-2, bit rates from 10 Kbit/s up to 5 Mbit/s, CAN termination selectable via jumper, electrical isolation (1000 V, 1 s)
CAN controller	esdACC in EP4CGX Altera FPGA, according to ISO 11898-1:2015
General:	
Ambient temp. Operation	0 °C ... +75 °C / Storage: -40 °C ... +85 °C
Rel. humidity	Max. 90 % (non-condensing)
Power supply	12 V, 2x CAN I _{MAX_12V} = 200 mA
Connector	CPCISerial: CompactPCI Serial connector P1, according to PICMG CPCI-S0 Rev. 1.0 CAN FD: DSUB9
Weight	150 g
Mechanics	3 U / 4 HP, compliant to IEEE 1101
LEDs	4x LED, CAN status, module status
Conformity	EN 61000-6-2, EN 61000-6-4, EMC, RoHS, CE

Order Information:

Hardware	Order No.
CPCISerial-CAN/402-2-FD 2x CAN FD via 2x DSUB9, 4 HP	1.3001.64

Software Support¹

CAN layer 2 drivers for Windows/Linux are included in delivery free of charge.

Additional CAN layer 2 object licenses including CD-ROM:

CAN-DRV-LCD QNX	Object Licence and CD for QNX6	C.1101.32
CAN-DRV-LCD RTX	Object Licence and CD for RTX64	C.1101.35
CAN-DRV-LCD VxWorks	Object Licence and CD for VxWorks	C.1101.55

Higher CAN layer protocols including CD-ROM for Classical CAN application:

CANopen-LCD Windows/Linux, QNX, RTX or VxWorks	C.1101.xx
J1939 stack for Windows, Linux, RTX	C.1130.xx
ARINC 825-LCD Windows/Linux, QNX, RTX, VxWorks	C.1140.xx

Related Products

CPCISerial-CAN/402-4-FD 4x CAN FD, DSUB25, 4 HP	1.3001.68
---	-----------

¹ For detailed information about driver availability for your operating system please contact our [sales team](mailto:sales@esd.eu).

CPC|serial-CAN/402-2-FD

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1:2015 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Test "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Supported bit rates from 10 kbit/s up to 5 Mbit/s
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)
- Busload measurement



Superior esdACC Features:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
 - Easy to program
 - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
 - Timestamping complies with the CiA 603 specification
- TX FIFO (16 CAN frames deep)
 - Providing the means to generate 100% busload even with non-realtime operating systems
 - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
 - High priority
 - 64 bit timestamp
 - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
 - e.g. for driver timeouts
 - ISO 11898-1:2015 conform
 - Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued)¹:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction relieves the host CPU (needs bus master capable local bus to host interface)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx® Spartan® and Altera® Cyclone FPGAs.

¹ Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.