CAN-USB/400

2x CAN (Layer 2, CANopen®, J1939 or ARINC 825)

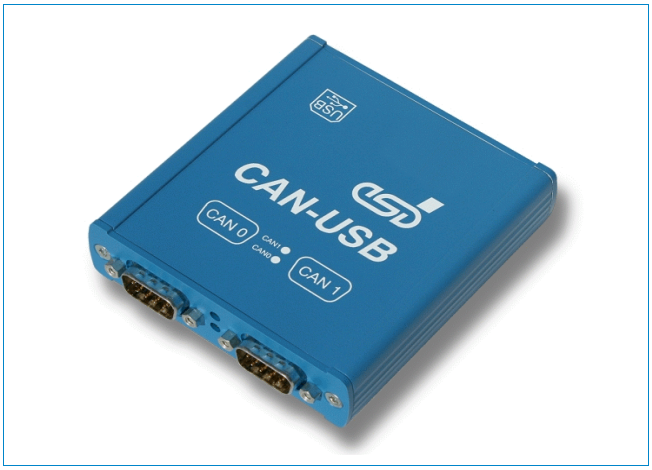
Two High-Speed CAN Interfaces for USB
- *CAN interfaces according to ISO 11898-2 with electrical isolation*
- *Powered by esd Advanced CAN Core (esdACC) implemented in an FPGA*
- *Capable of 100% CAN bus load*

Robust and Easy to Handle
- *Power supply by USB*
- *Aluminium case*
- *Incl. USB cable*

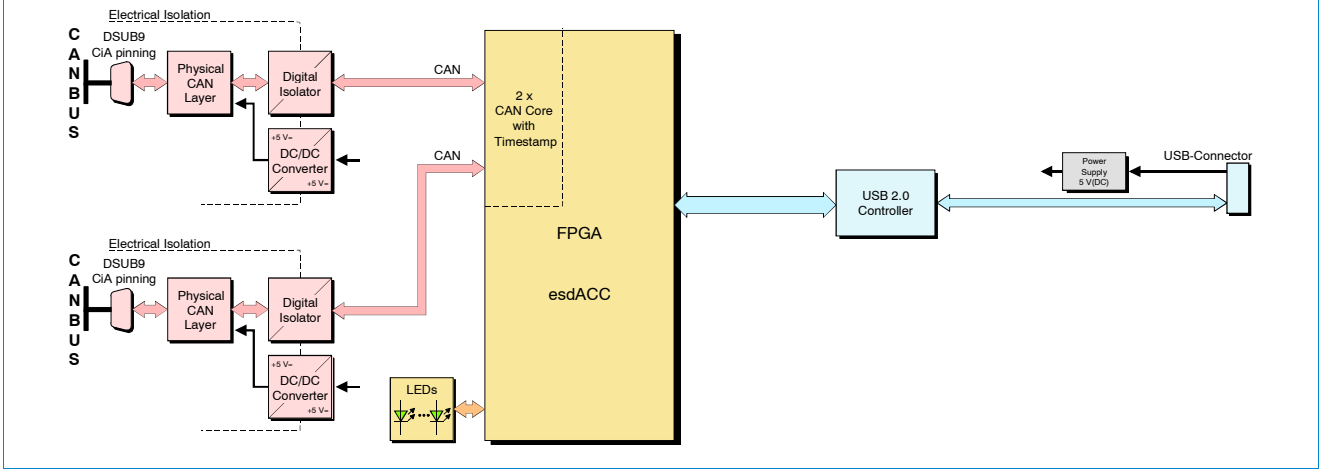
Advanced Diagnostics and Timestamping
- *Enhanced diagnostic features*
- *Error injection capabilities*
- *High resolution hardware timestamping*
- *CAN interfaces share common time base*

Optimized Architecture
Attached to USB via FIFO's and driven by esd Advanced CAN Core (esdACC), the CAN-USB/400 is designed for minimum latency CAN communication via USB.

Error Injection
A feature pretty unique on standard CAN interfaces. Error Injection provides means to simulate error conditions on CAN bus. Bit patterns can be injected into any living CAN bus. Several trigger conditions and modes are provided.



Software Support [1]
Operating system independent CAN layer 2 API (NTCAN)
- *Driver Support for Windows*
- *Multiple Higher Level Protocols available for Windows*
  - *CANopen Master- and Slave-Stack*
  - *J1939*
  - *ARINC825*
- *Drivers and software support for other operating systems are available on request.*



Technical Specifications:

USB Interface and Microprocessor:	
USB	*USB 2.0, high-speed 480 Mbit/s*
Memory	*BlockRAM: 72 KB*
CAN:	
Interface	*2x high-speed CAN interface acc. to ISO11898-2, bit rate 1 Mbit/s, differential, electrically isolated*
CAN controller	*esdACC in FPGA, acc. to ISO 11898-1*
General:	
Ambient temp.	*0 ...+50 °C*
Humidity	*Max. 90 %, non-condensing*
Supply voltage	*Via USB: 5 V*
Dimensions	*Approximately 86 mm x 19 mm x 86 mm (excl. connector excess length)*
Connectors	*CAN: 2x DSUB9 (male)* *USB: series B type (female)*

Order Information:		
Hardware		*Order No.*
CAN-USB/400	*2x CAN*	*C.2069.04*
CAN layer 2 drivers for Windows are included in delivery.		
Software Support		
CANopen object licences including CD-ROM [1]:		
	CANopen-LCD Windows	*C.1101.06*
J1939 stack for Windows including CD-ROM [1]:		
	J1939-LCD Windows	*C.1130.10*
ARINC 825 object licences including CD-ROM [1]:		
	ARINC825-LCD Windows	*C.1140.06*

1 For detailed information about the driver availability for your operating system please contact our sales team.

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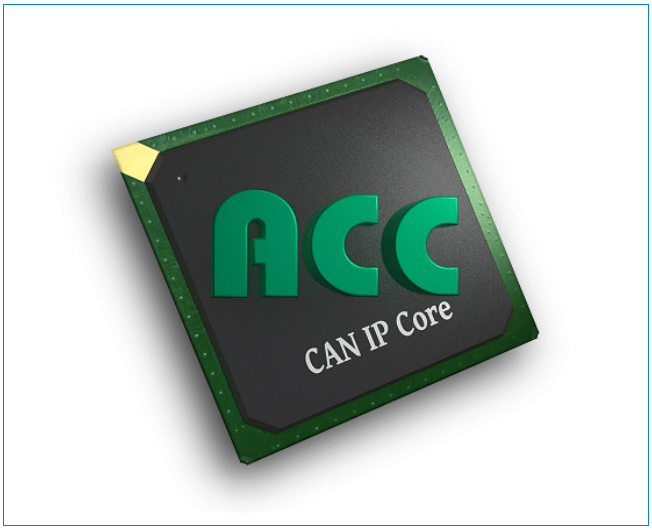
CAN-USB/400

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- 11-bit and 29-bit CAN IDs
- Bit rates from 10 kbit/s up to 1 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Single-shot transmission (no re-transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (software supported bit rate detection)
- Acceptance filter (4-byte code, 4-byte mask)
- Self reception mode (reception of 'own' messages)
- Busload measurement



Superior esdACC Features:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64 bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX
- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)

Superior esdACC Features (continued):

- Optional integration with 32-bit microcontroller to further relieve host CPU
- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.

For further information on the esdACC IP Core please contact our sales team.

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All data are subject to change without prior notice.

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