CAN-PCI/402-2-FD

2 Channel PCI-CAN FD Interface

PCI Board with High-Performance Intel® FPGA for 2x CAN FD

- *2 CAN FD interfaces according to ISO 11898-2, up to 8 Mbit/s*
- *Bus mastering and local data management by FPGA (esdACC)*
- *PCI interface according to PCI Local Bus Specification 3.0*
- *Selectable CAN termination on board*
- *Supports MSI (Message Signaled Interrupts)*

Wide Range of Operating System Support and Advanced CAN Diagnostic

- *Software drivers for Windows® and Linux® included free of charge*
- *Optional CAN layer 2 software drivers for real-time operating systems*
- *CANopen®, J1939 and ARINC 825 protocol libraries available for Classical CAN applications*
- *ISO 16845:2004 certified esd Advanced CAN Core (esdACC) technology*
- *High resolution hardware timestamps*

Advanced CAN Controller

- *esd ACC technology offers highest CAN performance and diagnostic*

Customization on Request

- *Low profile version for 1x or 2x CAN*
- *Ext. temperature range: -40°C … 75°C*
- *Error-simulation support*

CAN FD

The CAN-PCI/402-2-FD is a PC board designed for the PCI bus, that features two electrically isolated high-speed CAN FD interfaces according to ISO 11898-1:2015. The CAN FD interfaces are driven by the ISO 16845:2004 certified esdACC (esd advanced CAN Core) implemented in the Intel® FPGA.

With a higher bit rate in the data phase in combination with the increase of efficiency by a higher number of user-data bytes, CAN FD offers a higher data throughput while maintaining the benefits of Classical CAN. The CAN-PCI/402-2-FD is fully backwards compatible with CAN and can be also used in Classical CAN applications.

CAN Data Management

The FPGA supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions, in particular at higher data rates and a reduced host CPU load.

Due to the usage of MSI (Message Signaled Interrupts) the CAN-PCI/402-2-FD can be operated for example in Hypervisor environments. CAN-PCI/402-2-FD provides high resolution 64-bit hardware timestamps for CAN messages.

Software Support

Windows and Linux (NTCAN-API)
The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

Real-time OS (NTCAN-API)
CAN layer 2 drivers for QNX® and RTX64®, can be ordered separately, others on request.

Higher Layer Protocols
(Classical CAN application only)
Higher Layer Protocols are available for many operating systems (see order info):

- *CANopen Master- and Slave-Stack*
- *J1939*
- *ARINC825*

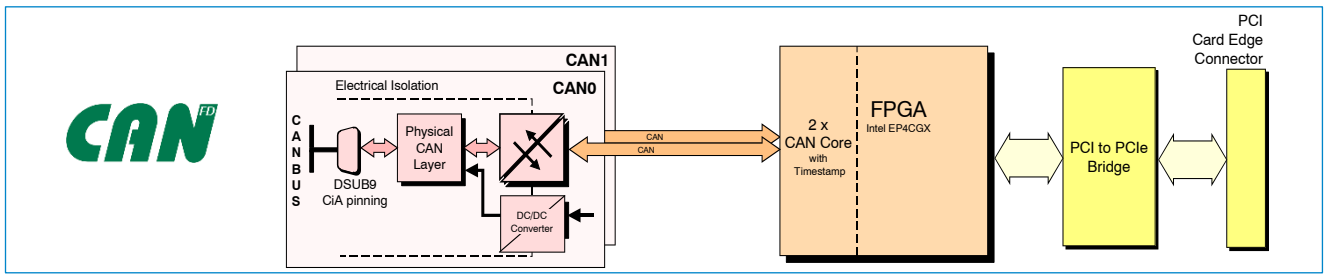
Additional free-of-charge esd CAN tools for Windows are downloadable from our website. The tools offer efficient setup and analysis of Classical CAN applications and networks.

Customization on Request

Customized options are available for customized series production in reasonable quantities. Please contact our sales team for detailed information.

Related Products

The CAN-PCI/402 is also available with up to four Classical CAN interfaces.
The CAN-PCIe/402-FD is designed as PCI Express® board.



Technical Specifications:

PCI Interface:	
Specification	*PCI 3.0, 32 bit, 33/66 MHz, 3.3 V (5 V tolerant), PCI bus master capability*
CAN:	
Interface	*2x CAN FD high-speed interfaces according to ISO 11898-2, with electrical isolation, bit rates from 10 Kbit/s up to 8 Mbit/s*
CAN controller	*esdACC in EP4CGX Intel FPGA, According to ISO 11898-1:2015*
General:	
Power supply	*3.3 V: 2x CAN I_{MAX} = 700 mA*
Ambient temp.	*0 °C ... +75 °C*
Rel. humidity	*Max. 90 % (non-condensing)*
Connector	*PCI: PCI card edge connector CAN: 1x 9-pin DSUB per CAN FD channel, pin contact*
Weight	*CAN-PCI/402-2-FD: 75 g*

Order Information:		
Hardware		*Order No.*
CAN-PCI/402-2-FD	*CAN interface board for PCI, 2 CAN FD interfaces acc. to ISO 11898-1:2015*	*C.2049.64*
Software Support [1]		
CAN layer 2 drivers for Windows/Linux are included in delivery free of charge. Additional CAN layer 2 object licences including CD-ROM:		
CAN-DRV-LCD QNX	*Object Licence and CD for QNX6*	*C.1101.32*
CAN-DRV-LCD RTX	*Object Licence and CD for RTX64*	*C.1101.35*
Higher CAN layer protocols including CD-ROM for Classical CAN Application:		
CANopen-LCD Windows/Linux, RTX, QNX or VxWorks[2]		*C.1101.xx*
J1939 stack for Windows, Linux, RTX		*C.1130.xx*
ARINC 825-LCD Windows/Linux, RTX, QNX[2], VxWorks[2]		*C.1140.xx*
Related Products		
CAN-PCI/402-2	*2x Classical CAN interfaces*	*C.2049.04*

1 For detailed information about driver availability for your operating system please contact our sales team.
2 Available on request

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CAN-PCI/402-2-FD

Driven by esdACC-FD (Advanced CAN Core)

Basic Product Features:
• CAN ISO 11898-1:2015 protocol compatibility
• Tested and certified acc. to ISO CAN Conformance Tests “ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan”
• 11-bit and 29-bit CAN IDs
• Supported bit rates: From 10 kbit/s up to 8 Mbit/s
• Receive buffer (64 CAN messages)
• Complete access to CAN error counters
• Programmable error warning limit
• Error code capture register
• Error interrupt for each CAN bus error
• Arbitration lost interrupt with detailed bit position
• Listen only mode (no acknowledge, no active error flags)
• Automatic bit rate detection (hardware supported bit rate detection)
• Self-reception mode (reception of ‘own’ messages)
• Busload measurement

Superior esdACC Features [1]:
• Operating system independently programmable via esd's NTCAN-API

• 32-bit register interface optimized for CAN needs
  • Easy to program
  • Transmission and reception of CAN frames with a minimum of register accesses

• RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  • Timestamping complies with the CiA 603 specification
  • On hardware with IRIG-B interfaces IRIG-B time is used for timestamping

• TX FIFO (16 CAN frames deep)
  • Providing the means to generate 100% busload even with non-real-time operating systems
  • Providing the means for real back-to-back transmission

• Timestamped Tx FIFO (16 CAN frames deep)
  • High priority
  • 64-bit timestamp
  • Bit time accuracy for CAN transmission

• Frame accurate abortion of transmissions with minimum delay
  • e.g. for driver timeouts
  • ISO11898-1:2015 conform
  • Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:
• Hardware timer to provide accurate software timeouts beyond operating system accuracy
• Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
• Optional different sources for timestamps (e.g. IRIG-B)
• Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
• The esdACC IP core has been verified on Xilinx® Spartan® and Intel® Cyclone® FPGAs.

[1] *Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.*

For further information on the esdACC IP Core please contact our sales team.

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