CAN-PCI/400

2 or 4 Channel PCI-CAN Interface (Layer 2, CANopen® or J1939)

PCI Board for up to 4xCAN

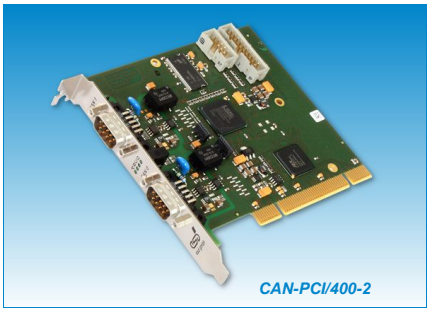
- 2x or 4x High-Speed CAN interfaces according to ISO 11898-2
- PCI bus according to PCI Local Bus Specification 2.2
- esd Advanced CAN Core (esdACC) technology
- Bus mastering and local data management by FPGA
- Software drivers for Windows® and Linux® included free of charge

Real-time OS Support and Higher Layer Protocols CANopen, J1939, ARINC825

- Software Drivers for Windows®, Linux®, VxWorks®, QNX®, RTX, On Time RTOS-32 and others
- CANopen®, J1939 and ARINC 825 protocol libraries are available

Advanced CAN Diagnostics

- Enhanced diagnostic features
- Error injection capabilities
- High resolution hardware timestamping



Powerful CAN Interface for PCs

The CAN-PCI/400 is a PC board designed for the PCI bus that features two(CAN-PCI/400-2) or optionally four (CAN-PCI/400-4) electrically isolated CAN High-Speed interfaces according to ISO11898-2. CAN-PCI/400-4 comes with two CAN interfaces via a separate slot bracket.

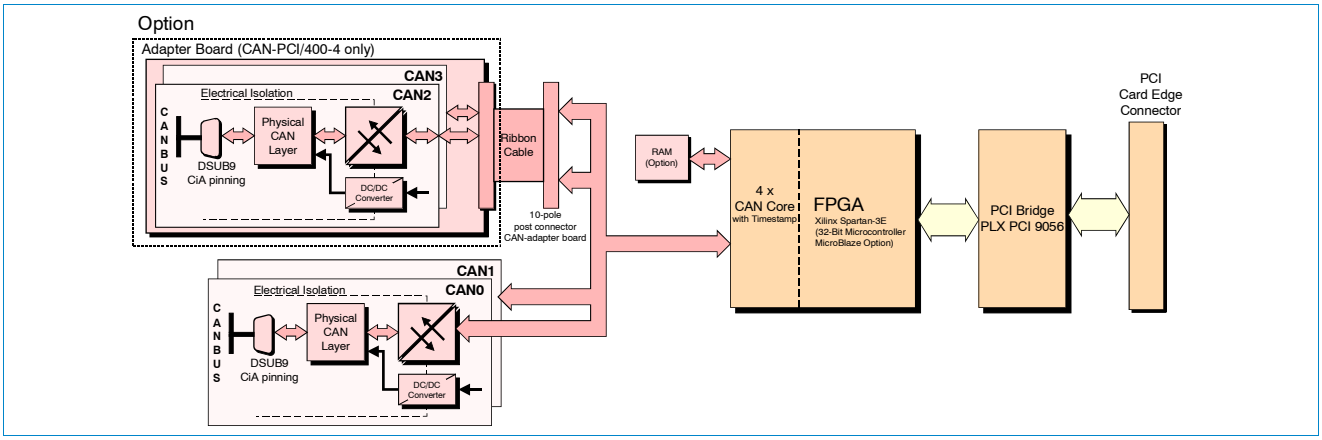
CAN Data Management

The independent CAN nets acc. to ISO11898-1 are driven by the esdACC (esd Advanced CAN Core) implemented in the Xilinx® Spartan®-3E FPGA.
Controlled by the FPGA the CAN-PCI/400 supports bus mastering as an initiator, meaning that it is capable of initiating write cycles to the host CPU's RAM independent of the CPU or the system DMA controller. This results in a reduction of overall latency on servicing I/O transactions in particular at higher data rates and reduced host CPU load. The CAN-PCI/400 provides high resolution 64 bit hardware timestamps with bit time accuracy.
CAN Error injection.

Software Support

CAN layer 2 (NTCAN-API) software drivers are available for Windows, Linux, RTX and RTX64, VxWorks, QNX, and On Time RTOS-32.

Additional free-of-charge esd CAN tools for Windows are downloadable from our website. The tools offer efficient setup and analysis of CAN applications and networks.



Technical Specifications:

PCI:	
Specification	PCI 2.2, 32 bit 33/66 MHz, 3.3 V (5 V tolerant), PCI bus master capability
Memory	BlockRAM: 72 KB, DDR-SDRAM: 64 MB
Microprocessor	Optional 32-bit µC in FPGA (MicroBlaze)
CAN:	
Interface	2x or optional 4x CAN high-speed interfaces according to ISO11898-2, differential, electrically isolated, bit rate up to 1 Mbit/s
CAN controller	esdACC in FPGA Spartan®-3E, acc. to ISO 11898-1 (CAN 2.0 A/B)
General:	
Ambient temperature	0...50 °C
Relative humidity	Max. 90 % (non-condensing)
Connector	CAN: DSUB9 male, PCI: PCI card edge connector
LED	CAN traffic, power
Power Supply	3.3 V / (depending on FPGA-image, 2x CAN: up to I = 1 A), 5 V / 250 mA

Order Information:

Hardware		Order No.
CAN-PCI/400-2	2x CAN version	C.2048.04
CAN-PCI/400-4	4x CAN version	C.2048.06

CAN layer 2 drivers for Windows and Linux are included in delivery.

Software Support[1]

Additional CAN layer 2 object licences including CD-ROM:	
CAN-DRV-LCD QNX	C.1101.32
CAN-DRV-LCD VxWorks	C.1101.55
CAN-DRV LCD RTX (incl. RTX64)	C.1101.35
CAN-DRV-LCD On Time RTOS-32	C.1101.45
Higher CAN layer protocols including CD-ROM:	
CANopen-LCD Windows/Linux	C.1101.06
CANopen-LCD QNX	C.1101.17
CANopen-LCD VxWorks	C.1101.18
CANopen-LCD RTX	C.1101.16
J1939 stack for Windows (Object)	C.1130.10
J1939 stack for Linux (Object)	C.1130.11
J1939 stack for RTX (Object)	C.1130.12
ARINC825-LCD Windows/Linux	C.1140.06
ARINC825-LCD RTX	C.1140.16
ARINC825-LCD QNX	C.1140.17
ARINC825-LCD VxWorks	C.1140.18

[1] For detailed information about driver availability for your operating system please contact our sales team.

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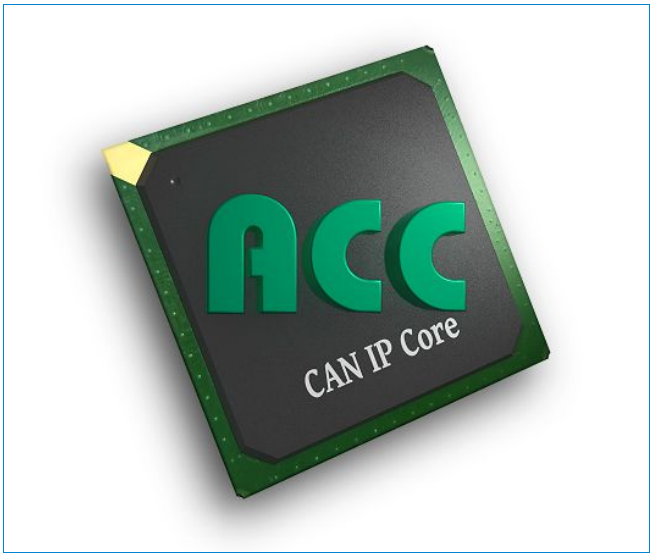
CAN-PCI/400

Driven by esdACC (Advanced CAN Core)

Basic Product Features:

- *CAN ISO 11898-1 protocol compatibility*
- *Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"*
- *11-bit and 29-bit CAN IDs*
- *Bit rates from 10 kbit/s up to 1 Mbit/s supported*
- *Receive buffer (64 CAN messages)*
- *Complete access to CAN error counters*
- *Programmable error warning limit*
- *Error code capture register*
- *Error interrupt for each CAN bus error*
- *Arbitration lost interrupt with detailed bit position*
- *Listen only mode (no acknowledge, no active error flags)*
- *Automatic bit rate detection (hardware supported bit rate detection)*
- *Acceptance filter (4-byte code, 4-byte mask)*
- *Self reception mode (reception of 'own' messages)*



Superior esdACC Features [1]:

- *Operating system independently programmable via esd's NTCAN-API*
- *32-bit register interface optimized for CAN needs*
  - *Easy to program*
  - *Transmission and reception of CAN frames with a minimum of register accesses*
- *RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 20.833 ns)*
  - *On hardware with IRIG-B interfaces IRIG-B time is used for timestamping*
- *TX FIFO (16 CAN frames deep)*
  - *Providing the means to generate 100% busload even with non-realtime operating systems*
  - *Providing the means for real back-to-back transmission*
- *Timestamped Tx FIFO (16 CAN frames deep)*
  - *High priority*
  - *64 bit timestamp*
  - *Bit time accuracy for CAN transmission*
- *Frame accurate abortion of transmissions with minimum delay*
  - *e.g. for driver timeouts*
  - *ISO11898-1 conform*
  - *Aborted frames in FIFO won't be blocked by low priority TX*

Superior esdACC Features (continued) [1]:

- *CAN error injection units*
  - *Simulating a wide range of error situations on CAN bus, e.g.:*
    - *ID pollution (100% bus load on certain CAN ID/priority)*
    - *Defective sensor (Destroying all CAN messages of a given CAN ID)*
  - *Different trigger modes*
    - *Bit pattern match*
    - *Time triggered*
    - *Immediate regarding CAN arbitration*
    - *External*
  - *'Cross CAN bus triggering' (event on one CAN bus triggers event on another bus)*
- *Hardware timer to provide accurate software timeouts beyond operating system accuracy*
- *Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)*
- *Optional integration with 32-bit microcontroller to further relieve host CPU*
- *Optional different sources for timestamps (e.g. IRIG-B)*
- *Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content*
- *The esdACC IP core has been verified on Xilinx Spartan and Altera Cyclone FPGAs.*

[1] *Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.*

For further information on the esdACC IP Core please contact our sales team.

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