# CPCI-CPU/750

# **CompactPCI-Controller Board with CAN and Giga-ETHERNET**



Hardware Manual

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#### Changes in the chapters

The changes in the document listed below affect changes in the  $\underline{\text{hardware}}$  as well as changes in the  $\underline{\text{description}}$  of the facts, only.

Chapter	Changes as compared with previous version
-	First issue
-	-

Technical details are subject to change without further notice.

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#### 1. Overview

#### 1.1 Description of the CPCI-CPU/750

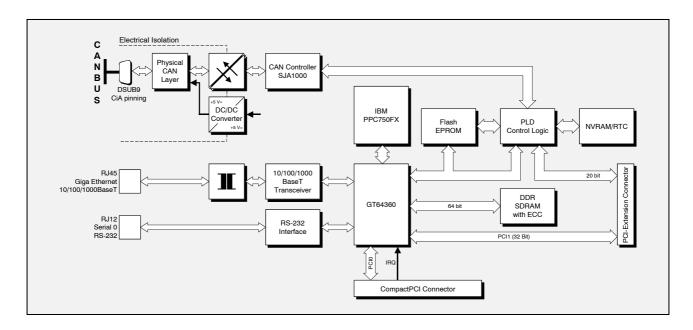


Figure 1.1.1: Block circuit diagram

The CPCI-CPU/750 is a CompactPCI board in Euro format. It is available as PCI-master CPU or as intelligent Slave board.

Apart from a powerful CPU the PowerPC processor PPC750FX has got a DDR-SDRAM controller with error correction (ECC), a PCI-bus interface and a PCI-extension connector, a serial interface, a CAN-bus interface and a MII interface as Giga-Ethernet interface.

The equipment of the CPCI-CPU/750 comprises a Flash-EPROM and up to 512 Mbyte DDR-SDRAM as memory and an RTC as timer with 32 Kbyte battery backed RAM.

The serial interface is designed as RS-232 interface. It is easily accessible via an RJ12-socket in the front panel.

The CAN interface is also accessible via the front panel. It is controlled via a CAN controller SJA1000. The interface is designed according to ISO11898, is electrically isolated and can be used for transmission rates of up to 1 Mbit/s.

The PCI-bus interface PCI0 is the CompactPCI-bus interface. The second PCI-bus interface PCI1 is accessible via a PCI-extension connector which is located directly on the board.

The Giga-Ethernet interface is suitable for 10, 100 and 1000 Mbit/s networks. They are connected via a RJ45 socket in the front panel.

The status of the module is displayed via LEDs in the front panel.



#### 1.2 PCB View

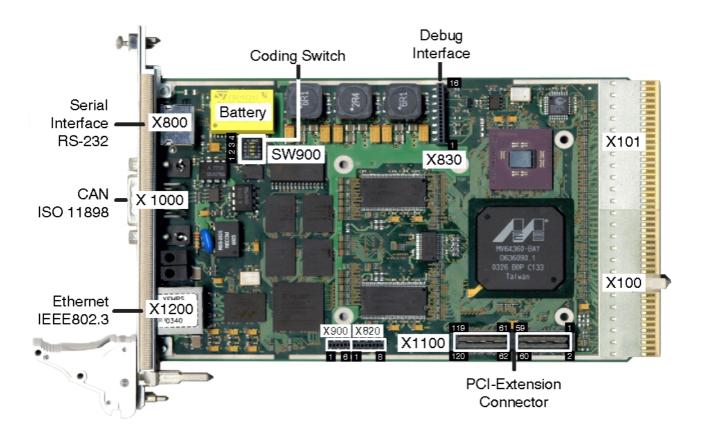


Figure 1.2.1: PCB view without cooling element

## 1.3 Summary of Technical Data

#### 1.3.1 General Technical Data

Ambient temperature	050 °C
Humidity	max. 90 %, non-condensing
Power supply	via CompactPCI bus, typically: $5 \text{ V} \pm 5\% / 3 \text{ A}$ and $3.3 \text{ V} \pm 5\% / 600 \text{ mA}$
Connectors	X100 (132-pole post connector) - CompactPCI-board connector J1 (PCI0) X101 (132-pole post connector) - CompactPCI-board connector J2 (PCI1) X800 (6-pole RJ12 socket) - RS-232 interface X830 (16-pole SMD socket strip) - Debug interface X1000 (9-pole DSUB connector) - CAN (ISO11898) X1100 (120-pole PCI-extension connector) - PCI-bus PCI1 X1200 (8-pole RJ45 socket, COMBO connector) - Ethernet Twisted Pair (IEEE 802.3)  For esd-internal programming and test purposes: X820 (8-pole SMD socket strip) - JTAG for MV64360 X900 (6-pole SMD socket strip) - JTAG for XCR 3256
Dimensions	100 mm x 160 mm
Weight	220 g

Table 1.3.1: General technical data



#### 1.3.2 CompactPCI Bus PCI0

Host bus	PCI bus according to PCI Local Bus Specification 2.2
PCI-data/address bus	64 bit
Controller	MV 64360
Interrupt	interrupt signal A, B, C, D
Board dimension	in accordance with CompactPCI-Specification, Release Note for PICMG 2.0 Revision 3.0
Connectors	
Connector coding	Universal-Board, not keyed (3.3 V or 5 V signalling voltage)

**Table 1.3.2:** CompactPCI-Bus interface PCI0

#### 1.3.3 PCI-Bus Extension PCI1

Host-bus	PCI-Bus according to PCI Local Bus Specification 2.2
PCI-data/address-bus	32 bit
Controller	MV 64360
Interrupt	interrupt signal A, B, C, D
Connectors	PCI-extension connector

Table 1.3.3: PCI-Bus interface PCI1



#### 1.3.4 Microprocessor and Memory

CPU	PPC750FX / 733 MHz (max. 800 MHz) / 64 bit
RTC / NVRAM	RTC with 32 K x 8 bit battery backed RAM or optional: 32 K x 8 bit NVRAM
Flash-EPROM	up to 32 M x 16 bit (64 Mbyte)
Serial-EEPROM	1 Kbyte
DDR-SDRAM	16 M x 64 bit (256 Mbyte) (default) from 8 M x 64 bit (64 Mbyte) (optional) up to 64 M x 64 bit (512 Mbyte) (optional)

**Table 1.3.4:** Microprocessor and memory

#### 1.3.5 Serial Interface

Controller	MV64360
Bit rate	MPSC: 300 bit/s 115.200 bit/s RS-232-transceiver: max. 115.200 bit/s
Physical interface	RS-232C
Connector	6-pole RJ12-socket in the front panel

**Table 1.3.5:** Serial interface

#### 1.3.6 CAN interface

CAN controller	SJA1000
CAN protocol	CAN 2.0A/2.0B
Physical interface	differential, connection in accordance with ISO 11898
Bit rate	10 Kbit/s 1 Mbit/s
Bus termination	has to be set externally
Connector	DSUB9-connector in the front panel

**Table 1.3.6:** CAN interface



#### 1.3.7 Ethernet Interface

Number	1
Bit rate	10 Mbit/s, 100 Mbit/s, 1000 Mbit/s
Controller	MV 64360
Physical interface	Twisted Pair (IEEE802.3) 10/100/1000BaseT
Electrical isolation	via transformer integrated in the connector
Connector	8-pole RJ45 socket in the front panel

**Table 1.3.7:** Ethernet interface

#### 1.3.8 Clock (RTC)

Function	time and calendar (M48T35K)
Battery	battery e.g.: Snaphat, M4T28 type BR12 SH1

Table 1.3.8: Clock

#### 1.3.9 Software support

The boot monitor U-Boot\* is stored in the Flash memory. Therefore it is possible for the CPCI-CPU/750 to boot with various operating systems from the network or the local Flash memory.

The operating systems Linux and VxWorks are available with corresponding drivers for the local interfaces. Further operating systems are available on request.

Furthermore the CAN-transmission protocols CANopen and a local WEB-server are available.

<sup>\*</sup> http://sourceforge.net/projects/u-boot/

#### 1.3.10 Order information

Туре	Properties	Order No.
CPCI-CPU/750	IBM PPC750FX, 733 MHz, 256 MB DDR-SDRAM, 64 MB Flash, CPCI- <i>Host</i> Adapter	I.2402.02
CPCI-CPU/750-VxW	VxWorks BSP/Adaption	I.2402.31
CPCI-CPU/750-Linux	Linux BSP/Adaption	I.2402.32
CPCI-CPU/750-MD	User manual in English <sup>1*)</sup> (this manual)	I.2402.21
CPCI-CPU/750-ENG	Engineering Manual in English <sup>2*)</sup> Contents: Circuit diagrams, PCB top overlay drawing, data sheets of significant components, but without MV64360 manual, which is available from Marvell only under NDA (Non-Disclosure-Agreement)	1.2402.25

<sup>1\*)</sup> If module and manual are ordered together, the manual is free of charge. 2\*) This manual is liable for costs, please contact our support.

Table 1.3.9: Order information



#### 2. Hardware Installation / Maintenance

#### 2.1 Hardware Installation

#### Attention!

Electrostatic discharges may cause damage to electronic components. To avoid this, please perform the following steps *before* you touch the CPCI-CPU/750 module, in order to discharge the static electricity from your body:

- Switch off the power of your CompactPCI system, but leave it connected to the mains.
- Please touch the metal case of the system now to discharge yourself.
- Furthermore, you should prevent your clothes from touching the CPCI module, because your clothes might be electrostatically charged as well.

#### Installation:

- Switch off your CompactPCI system and all connected peripheral devices (monitor, printer etc.).
   Switch off the other participants to whose CAN-network or serial interface the CPCI-CPU/750 module is to be connected.
- 2. Discharge your body as described above.
- 3. Connect the PCI-bus PCI1 via the PCI-extension connector (see page 4) on the module if necessary.
- 4. Select a free CompactPCI-bus slot and insert the CPCI-CPU/750 module. The module fits into any 3 HE CompactPCI bus slot.
- 5. Fix the module with the mounting screws in the front panel.
- 6. Connect the CAN-bus (X1000), Ethernet (X1200) and Serial (X800) interface. Please note that the CAN has to be terminated at both ends. **esd** offers T-connectors and terminations for this. Furthermore, the CAN-GND signal must be earthed at *exactly one* point in the CAN network. The termination connectors have a ground contact, therefore. A CAN user whose CAN interface is not electrically isolated acts as an earth connection.
- 7. Switch on the power supply of the CompactPCI system, the peripheral devices and the other CAN participants.
- 8. End of hardware installation.



#### **Demounting:**

- A1. Switch off the CompactPCI system and if necessary other network participants. Disconnect the connectors in the front panel.
- A2. Discharge your body as described above.
- A3. Unfasten the mounting screws in the front panel.
- A4. Unfasten the CPCI-CPU/750 by activating the eject lever and pull the module carefully out of the slot.
- A5. Remove the PCI-extension if necessary.

#### 2.2 Change of Battery:

The CPCI-CPU/750 comes with a RTC (Real Time Clock), which is energised with a battery. The battery is plugged in a holder directly on the board.

Battery type: e.g. Snaphat, Lithium battery M4T28 BR12 SH1.

- 1. Demount the module as described above.
- 2. Remove the old battery carefully out of the holder (see figure 1.2.1) and insert the new battery.
- 3. Install the module as described under 'Installation' on page 10.



## 3. Front Panel View with LED Display

The module has got four LEDs in the front panel.

#### 3.1 LEDs in the Front Panel

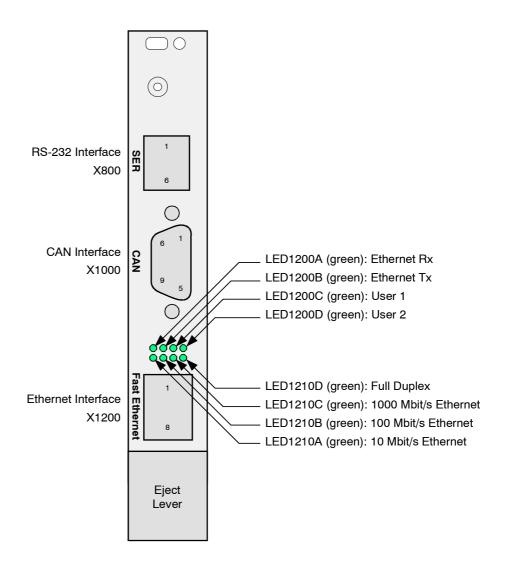


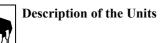
Figure 3.1.1: Position and colour of the LEDs



## 3.2 Display Functions of the LEDs

LED	Name	Meaning of LED when on
LED1200A	LED Rx	Receive status Ethernet (reception of Ethernet data packets)
LED1200B	LED TX	Transmit status Ethernet (transmission of Ethernet data packets)
LED1200C	USER LED 0	User-defined, display according to register entry
LED1200D	USER LED 1	User-defined, display according to register entry
LED1210A	LED Link 10	Ethernet bit rate: 10 Mbit/s
LED1210B	LED Link 100	Ethernet bit rate: 100 Mbit/s
LED1210C	LED Link 1000	Ethernet bit rate: 1000 Mbit/s
LED1210D	Full Duplex	Full Duplex operation

 Table 3.1.1: Display functions of the LEDs



## 4. Description of Units

#### 4.1 PowerPC Microcontroller PPC750FX

#### 4.1.1 General

The general functions of the PowerPC 750FX will not be explained in this manual. The manual of the microcontroller can be downloaded from the homepage of the manufacturer IBM, at:

http://www-3.ibm.com/chips/products/powerpc/processors/

#### 4.1.2 Address Assignment

Start address [HEX]	End address [HEX]	Unit
0x0000_0000	0x03FF_FFFF	DDR-SDRAM with 8 M x 64 bit (64 Mbyte) (72 bit for ECC)
0x0000_0000	0x1FFF_FFFF	DDR-SDRAM with 64 M x 64 bit (512 Mbyte), (72 bit for ECC)
0x8000_0000	0x87FF_FFFF	PCI0 memory space
0x8800_0000	0x8FFF_FFFF	PCI1 memory space
		Internal periphery:
0xF000_0000	0xF00F_FFFF	CS3 - NVRAM (8 bit)
0xF010_0000	0xF01F_FFFF	CS3 - register Reg0 (8 bit)
0xF020_0000	0xF02F_FFFF	CS3 - register Reg1 (8 bit)
0xF030_0000	0xF03F_FFFF	CS3 - register Reg2 (8 bit)
0xF040_0000	0xF0EF_FFFF	CS3 - reserved, not used (8 bit)
0xF0F0_0000	0xF0FF_FFFF	CS3 - CAN controller (SJA1000) (8 bit)
0xF100_0000	0xF107_FFFF	register in MV64360
0xF108_0000	0xF01B_FFFF	SRAM in MV64360
0xFA00_0000	0xfAFF_FFFF	PCI0 I/O-space (CPCI bus)
0xFB00_0000	0xfBFF_FFFF	PCI1 I/O-space (extension connector)
0xFC00_0000	0xFCFF_FFFF	CS0 (16 bit Flash)
0xFD00_0000	0xFDFF_FFFF	CS1 (16 bit Flash)
0xFE00_0000	0xFEFF_FFFF	CS2 (16 bit Flash)
0xFF00_0000	0xffff_ffff	CS-Boot (16 bit Flash)

**Table 4.1.1:** Address ranges

The table contains the default assignment of the registers. It can be changed by writing on the configuration registers of the PowerPC 750FX.

#### **Description of the Units**



#### 4.1.2.1 Register Reg0-Reg2

The bits of the registers are assigned as described below:

**Register Reg0** (0xF010\_0000 - 0xF01F\_FFFF):

access: read, write

Bit No.	7	6	5	4	3	2	1	0
Data content	WD0	WDEN (Set only!)	0	0	0	0	ULED1	ULED0

Description of the bits: WD0 => if WDEN =1, the content of WD0 has to be toggled every

500 ms, otherwise *Reset* of the board

WDEN = 0 -> Watchdog disabled, =1 -> Watchdog enabled

can only be set to '1', setting to '0' only with Reset

ULEDx =  $0 \rightarrow \text{LED off}$ , =  $1 \rightarrow \text{LED on } (x = 0,1)$ 

Default after Reset, all bits = 0

**Register Reg1** (0xF020\_0000 - 0xF02F\_FFFF):

access: read

Bit No.	7	6	5	4	3	2	1	0
Data content	1	1	1	1	1	IRQ2	IRQ1	CANIRQ

description of the bits: IRQx =  $0 \rightarrow IRQ$  active, =  $1 \rightarrow no$  IRQ (x = 0,1)

CANIRQ =  $0 \rightarrow IRQ$  active, =1  $\rightarrow$  no IRQ

**Register Reg2** (0xF030\_0000 - 0xF03F\_FFFF):

access: read

Bit No	7	6	5	4	3	2	1	0
Data content	H ()	0	0	0	CFG3	CFG2	CFG1	CFG0

Description of the bits: CFGx = 0 ->coding switches on, =1 ->coding switches off

(x = 0-3)

#### 4.2 Serial Interface

#### **4.2.1 Default Setting**

The default setting of the serial interface is:

Bit rate: 9600 Baud

Data bits: 8
Parity: no
Stop bits: 1

Handshake: XON/XOFF

#### **4.2.2** Configuration

The serial interface is controlled by MPSC0 in the MV 64360. The bit rate of the interface can be configured per software. The MPSC in the MV 64360 used as UART and the RS-232 driver of the interface support bit rates of up to 115.2 Kbit/s.

The procedure to change the bit rate depends on the operating system, it is therefore advisable to refer to the manual of the operating system.



#### 4.2.3 Connection of the RS-232 Interface

The diagram is used to explain the short terms for signals as used in the chapter connector assignments. The signal terms are exemplary for the connection of the CPCI-CPU/750 as a modem (DCE) via the adapter cable RJ12-DSUB9.

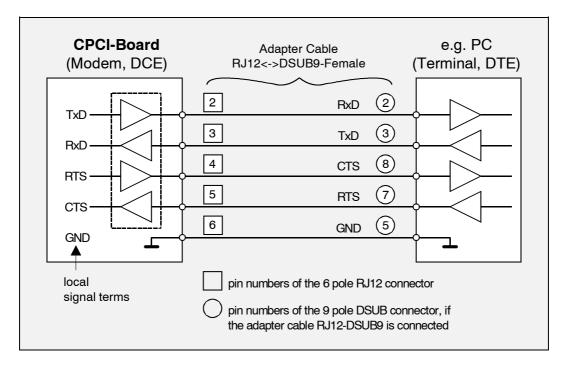


Figure. 4.2.1: Connection diagram for RS-232 operation

#### 4.3 Function of the Coding Switch

#### 4.3.1 Overview

Coding switch bit	Function	Default setting at delivery
1	has not yet been defined	-
2	has not yet been defined	-
3	has not yet been defined	-
4	switching the boot Flash-EPROM	boot from Flash-EPROM U720

**Table 4.3.1:** Assignment of coding switch bits

#### 4.3.2 Switching the Boot-Flash-EPROM via Coding Switch Bit 4

The local operating system is booted from the Flash-EPROM U720 per default (Chip-Select CS-Boot des MV64360). By means of the coding switch the chip select signal can be switched so that the Flash-EPROM U730 will be accessed. With coding switch bit 4 both Flash-EPROMS can be 'interchanged'.

This switching can be used, for instance, to boot an 'Emergency Operating System' in the second Flash EPROM, if the board does not boot up again after a change in the default Flash-EPROM.

Position of coding switch bit 4	Function
1	Memory range of the Flash-EPROMs: U730 on CS-Boot U720 on CS2
0	Memory range of the Flash-EPROMs: U730 on CS2 U720 on CS-Boot (default setting)

**Table 4.3.2:** Meaning of coding switch bits 4

After a hardware reset the address 0xFFF0\_0100 CS boot will be shown. The processor starts the execution of the program there.



#### 4.4 CAN Unit

#### 4.4.1 General

The CAN interface of the CPCI-CPU/750 is controlled by the CAN controller SJA1000.

The CAN interface is easily accessible via the 9-pin DSUB connector X1000 in the front panel. A 82C250/82C251 is used as driver unit. The differential CAN bus signals are electrically isolated from other potentials.

#### **4.4.2** Interface Circuits

The figure below shows the principal circuit of the CAN interface.

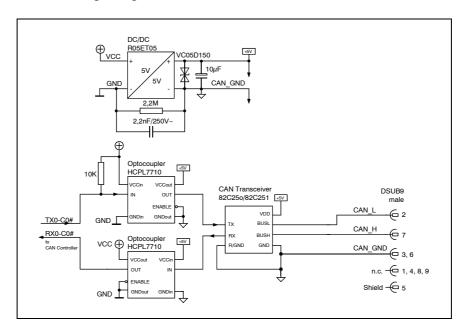


Figure. 3.4.1: Circuit of the CAN interface



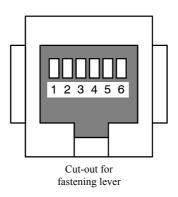
## 5. Connector Assignment

#### **5.1 Serial Interface**

For details on the connection of serial interfaces please refer to chapter 'Serial Interfaces' on page 17. From the principle circuit diagrams represented in that chapter, you will be able to clearly determine the signal direction (Rx<->Tx).

#### 5.1.1 Assignment of the RJ12 socket X800

#### **Pin Position:**

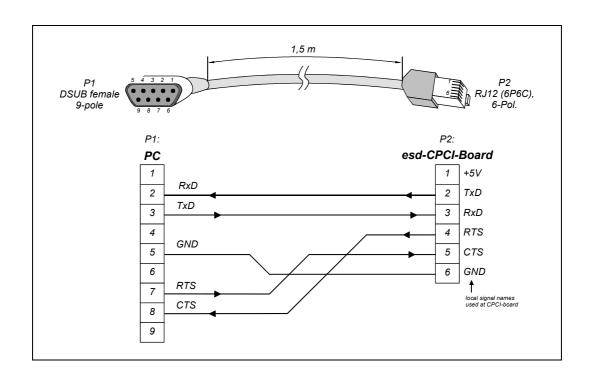


**Pin Assignment:** 

Pin	Signal
1	+5 V
2	TxD Data Output
3	RxD Data Input
4	RTS Handshake Output
5	CTS Handshake Input
6	GND

The data direction of the signals is given as viewed from the CPCI-CPU/750 board.

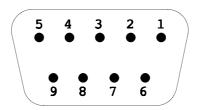
#### 5.1.2 Connection Cable RJ12-DSUB9





#### 5.1.3 DSUB9-Socket when using the Adapter Cable RJ12-DSUB9

#### **Pin Position:**



#### Pin Assignment:

S	Signal		in	Signal	
n.c.		1			
RxD	(Output)	2	6	n.c.	
KXD	(Output)		7	RTS	(Input)
TxD	(Input)	3	,	KID	(Input)
	( 1 )		8	CTS	(Output)
n.c.		4			<u> </u>
GND		5	9	n.c.	

9-pin DSUB socket n.c. ... not connected

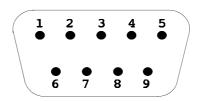
The Signal names are specified as viewed from the terminal (PC). The signal direction specified in brackets is shown as viewed from the CPCI-CPU/750 board.



#### **5.2 CAN Bus Interface (X1000)**

The DSUB9 Connector (X1000) of the CAN interface is located in the front panel of the CPCI-CPU/750.

#### **Pin Position:**



#### **Pin Assignment:**

Signal	Pin		Pin		Signal
G.1.1. G.1.5		1	reserved		
CAN_GND	6	2	CAN L		
CAN H	7	2	CAN_L		
_	0	3	CAN_GND		
reserved	8	4	reserved		
reserved	9	Т	10301 VCu		
15552.54		5	Shield		

<sup>9-</sup>pole DSUB connector

#### **Signal Description:**

CAN\_L, CAN\_H... CAN-Signal lines

CAN\_GND ... reference potential of the local CAN-physical layers

Shield ... potential of the connector case

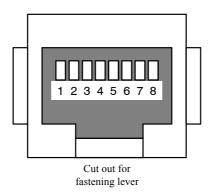
reserved ... reserved for future applications



## **5.3 ETHERNET 10/100/1000BaseT Connection (X1200)**

The RJ45 socket (X1200) of the Ethernet interface is easily accessible via the front panel of the CPCI-CPU/750.

#### **Pin Position:**



Pin Assignment:

Signal
MDI0+
MDI0-
MDI1+
MDI2+
MDI2-
MDI1-
MDI3+
MDI3-

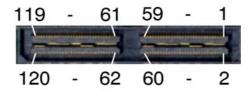
8-pole RJ45 socket

For the operation with bit rates of 10 Mbit/s and 100 Mbit/s only the signals MDI0 and MDI1 are used.



## 5.4 Additional PCI-Bus Interface PCI1 (X1100)

PCI-extension for Add-On-cards



Connector type: PCI-Extension connector QSH-060-01-F-D-A of Samtec

Signal	Pin	Pin	Signal
3,3 V	61	62	GND
3,3 V	63	64	GND
C/BE3#	65	66	AD22
AD24	67	68	AD23
AD27	69	70	AD25
AD28	71	72	AD26
GND	73	74	VIO
GND	75	76	VIO
AD29	77	78	AD31
AD30	79	80	CLK0
GND	81	82	VCC
GND	83	84	VCC
TX-S1/GNT0#	85	86	CLK1
RX-S1/GNT1#	87	88	RST#
RTS-S1/REQ0#	89	90	INTA#
CTS-S1/REQ1#	91	92	INTB#
GND	93	94	INTC#
GND	95	96	INTD#
GND	97	98	VCC
GND	99	100	VCC
RES0	101	102	RES10
RES1	103	104	RES11
RES2	105	106	RES12
RES3	107	108	RES13
RES4	109	110	RES14
RES5	111	112	RES15
RES6	113	114	RES16
RES7	115	116	RES17
RES8	117	118	RES18
RES9	119	120	RES19

Signal	Pin	Pin	Signal
VCC	1	2	GND
VCC	3	4	GND
3,3 V	5	6	-12 V
3,3 V	7	8	+12 V
AD04	9	10	AD00
AD05	11	12	AD01
VCC	13	14	VIO
VCC	15	16	VIO
AD08	17	18	AD02
AD11	19	20	AD03
GND	21	22	3,3 V
GND	23	24	3,3 V
M66EN	25	26	AD06
C/B0#	27	28	AD07
3,3 V	29	30	GND
3,3 V	31	32	GND
AD12	33	34	AD09
AD14	35	36	AD10
AD15	37	38	AD13
C/BE1#	39	40	PERR#
PAR	41	42	VIO
SERR#	43	44	VIO
STOP#	45	46	IRDY#
DEVSEL#	47	48	TRDY#
GND	49	50	3,3V
GND	51	52	3,3V
FRAME#	53	54	AD16
C/BE2#	55	56	AD17
AD19	57	58	AD18
AD20	59	60	AD21



#### 5.5 Debug-Port at X830

With the debug port e.g. firmware can be updated. It can be connected via a SMD-pin contact strip connector. It is recommended to build a simple adapter from the 16-pole SMD-pin contact strip connector to a 16-pin post connector to connect the port.

**Attention:** The SMD-pin contact strip connector has no polarity! Take care to insert it into the correct position. The orientation of the pins of X830 is shown on page 4.

Signal assignment of the 16-pole SMD socket strip and JTAG adapter

to X830 16-pole SMD-Strip

1	IDO	1
<u> </u>	QACK#	
2	TDI	3
3	TRST#	
4	QREQ#.	4
5	2k2 Pull-Up to 2.5V	5
6	TCK	6
7	CKSTPI#	7
8		8
9	TMS	9
10	n.c.	10
_	SRST#	11
11	GND	
12	HRST#	12
13	n.c.	13
14	CKSTPO#	14
15	GND	15
16	GND	16

JTAG Connector 16-pole Post Connector



example of an adapter (uncasted)

**Connectors to build the adapter:** SMD

SMD-pin contact strip:

by Samtec, 'modified pin contact strip', order-no. MTMS-116-52-T-S-185

Post connector:

e.g. by Harting, 16-pole, straight, order-no. 09185167324

# Connector Assignment

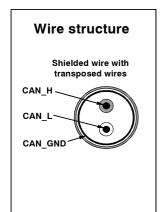
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## 6. Correctly Wiring Electrically Isolated CAN Networks

Generally all instructions applying for wiring regarding an electromagnetic compatible installation, wiring, cross sections of wires, material to be used, minimum distances, lightning protection, etc. have to be followed.

The following **general rules** for the CAN wiring must be followed:

1.	A CAN net must not branch (exception: short dead-end feeders) and has to be terminated by the wave impedance of the wire (generally 120 W $\pm 10\%$ ) at both ends (between the signals CAN_L and CAN_H and <b>not</b> at GND)!		
2.	A CAN data wire requires <b>two twisted</b> wires and a wire to conduct the reference potential (CAN_GND)!  For this the shield of the wire should be used!		
3.	The reference potential CAN_GND has to be connected to the earth potential (PE) at <b>one</b> point. Exactly <b>one</b> connection to earth has to be established!		
4.	The bit rate has to be adapted to the wire length.		
5.	Dead-end feeders have to kept as short as possible (I < 0.3 m)!		
6.	When using double shielded wires the external shield has to be connected to the earth potential (PE) at <b>one</b> point. There must be not more than <b>one</b> connection to earth.		
7.	A suitable type of wire (wave impedance ca. 120 $\Omega$ ±10%) has to be used and the voltage loss in the wire has to be considered!		
8.	CAN wires should not be laid directly next to disturbing sources. If this cannot be avoided, double shielded wires are preferable.		



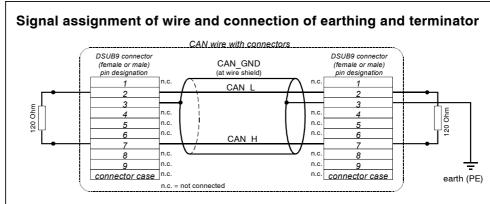
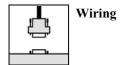


Figure: Structure and connection of wire



### **Cabling**

O for devices which have only one CAN connector per net use T-connector and dead-end feeder (shorter than 0.3 m) (available as accessory)

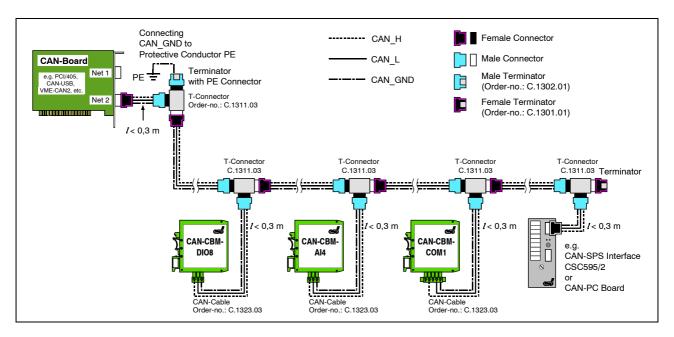


Figure: Example for correct wiring (when using single shielded wires)

#### **Terminal Resistance**

- O use **external** terminator, because this CAN later be found again more easily!
- O 9-pin DSUB-terminator with male and female contacts and earth terminal are available as accessories

#### **Earthing**

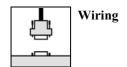
- O CAN\_GND has to be conducted in the CAN wire, because the individual esd modules are electrically isolated from each other!
- O CAN GND has to be connected to the earth potential (PE) at **exactly one** point in the net!
- O each CAN user without electrically isolated interface works as an earthing, therefore: do not connect more than one user without potential separation!
- O Earthing CAN e.g. be made at a connector

## Wire Length

Optical couplers are delaying the CAN signals. By using fast optical couplers and testing each board at 1 Mbit/s, however, esd CAN guarantee a reachable length of 37 m at 1 Mbit/s for most esd CAN modules within a closed net without impedance disturbances like e.g. longer dead-end feeders. (Exception: CAN-CBM-DIO8, -AI4 and AO4 (these modules work only up to 10 m with 1 Mbit/s))

Bit rate [Kbit/s]	Typical values of reachable wire length with esd interface l <sub>max</sub> [m]	CiA recommendations (07/95) for reachable wire lengths l <sub>min</sub> [m]
1000	37	25
800	59	50
666.6	80	-
500	130	100
333.3	180	-
250	270	250
166	420	-
125	570	500
100	710	650
66.6	1000	-
50	1400	1000
33.3	2000	-
20	3600	2500
12.5	5400	-
10	7300	5000

Table: Reachable wire lengths depending on the bit rate when using esd-CAN interfaces



## **Examples for CAN Wires**

Manufacturer	Type of wire	
U.I. LAPP GmbH Schulze-Delitzsch-Straße 25 70565 Stuttgart Germany www.lappkabel.de	e.g. UNITRONIC ®-BUS CAN UL/CSA UNITRONIC ®-BUS-FD P CAN UL/CSA	(UL/CSA approved) (UL/CSA approved)
ConCab GmbH Äußerer Eichwald 74535 Mainhardt Germany www.concab.de	e.g. BUS-PVC-C (1 x 2 x 0,22 mm²) BUS-Schleppflex-PUR-C (1 x 2 x 0,25 mm²)	Order No.: 93 022 016 (UL appr.) Order No.: 94 025 016 (UL appr.)
SAB Bröckskes GmbH&Co. KG Grefrather Straße 204-212b 41749 Viersen Germany www.sab-brockskes.de	e.g. SABIX® CB 620 (1 x 2 x 0,25 mm²) CB 627 (1 x 2 x 0,25 mm²)	Order No.: 56202251 Order No.: 06272251 (UL appr.)

Note: Completely configured CAN wires can be ordered from esd.