CAN-USB/400-FD

USB Module with 2 CAN FD Interfaces

Two High-Speed CAN FD Interfaces for USB
- CAN FD interfaces according to ISO 11898-2 with electrical isolation
- Powered by ISO 16845:2004 certified esd Advanced CAN Core (esdACC) implemented in an FPGA
- Capable of 100% CAN bus load

Robust and Easy to Handle
- Power supply by USB
- Aluminium case
- USB cable included
- High retention force USB connector

Advanced Diagnostics and Timestamping
- Enhanced diagnostic features
- Error injection capabilities
- High resolution hardware timestamping
- CAN interfaces share common time base

Customization on Request
- Analog and digital IRIG-B inputs

Optimized Architecture
Attached to USB via FIFO's and driven by esd Advanced CAN Core (esdACC), the CAN-USB/400-FD is designed for minimum latency CAN communication via USB.

CAN FD
The CAN-USB/400-FD comes with two independent CAN FD interfaces according to ISO 11898-1, which are driven by the ISO 16845:2004 certified esdACC (esd advanced CAN Core) implemented in an FPGA.
The interface is able to send and receive ISO conform CAN FD or CAN 2.0 A/B messages. The CAN FD bit rate range is validated for the esdACC CAN FD core from 10 kbit/s up to 8 Mbit/s.

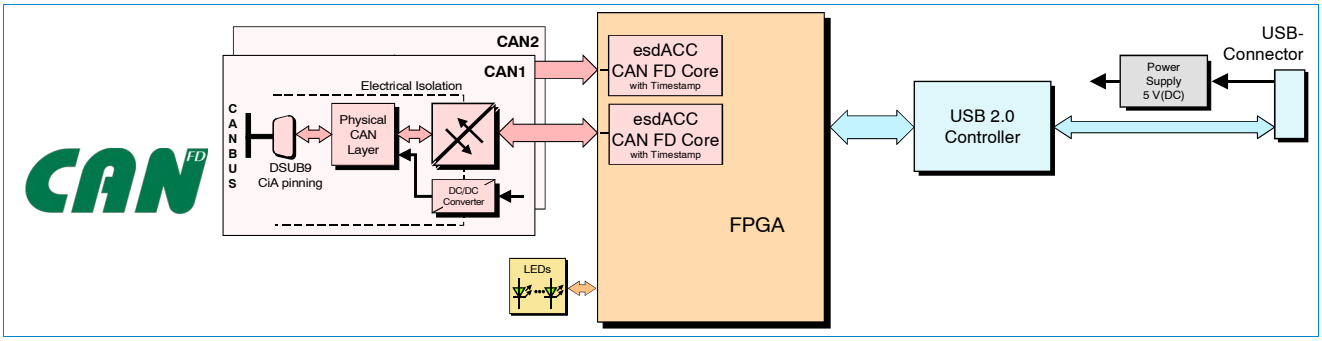
Error Injection
A feature pretty unique on standard CAN interfaces (Classical CAN application only). Error Injection provides means to simulate error conditions on CAN bus.
Bit patterns can be injected into any living CAN bus. Several trigger conditions and modes are provided.

Software Support
Windows (NTCAN-API)
The CAN layer 2 drivers for Windows are included in the scope of delivery.

Higher Layer Protocols
(Classical CAN application only)
Higher Layer Protocols are available for Windows (see order info):
- CANopen Master- and Slave-Stack
- J1939
- ARINC825

Additional free-of-charge esd CAN tools for Windows are downloadable from our website. The tools offer efficient setup and analysis of CAN applications and networks.

Customization on Request
Customized options are available for customized series production in reasonable quantities. Please contact our sales team for detailed information.



Technical Specifications:

USB Interface and Microprocessor:	
USB	USB 2.0, high-speed 480 Mbit/s
Memory	BlockRAM: 72 KB
CAN:	
Interface	2x high-speed CAN FD according to ISO11898-2, bit rates from 10 kbit/s up to 8 Mbit/s (with the same CAN transceiver), electrically isolated
CAN controller	esdACC in Cyclone® IV FPGA, according to ISO 11898-1
General:	
Ambient temperature	0 °C ... +50 °C
Rel. humidity	Max. 90 % (non-condensing)
Power supply	Via USB: 5 V
Dimensions	Approximately 86 mm x 19 mm x 86 mm (excl. connector excess length)
Connectors	CAN: 2x DSUB9 (pin contacts) USB: USB2 standard socket type-B, high retention force connector

Order Information:

Hardware		Order No.
CAN-USB/400-FD	2x CAN FD	C.2069.64

Software Support[1]

CAN layer 2 drivers for Windows are included in delivery free of charge.

Higher CAN layer protocols including CD-ROM for Classical CAN Application:

CANopen-LCD Windows	C.1101.06
J1939-LCD Windows	C.1130.10
ARINC825-LCD Windows	C.1140.06

Related Products

CAN-USB/400	2x CAN	C.2069.04
CAN-USB/400-IRIG-B	2x CAN, IRIG-B Input	C.2069.06

1 For detailed information about driver availability for your operating system please contact our sales team.

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CAN-USB/400-FD

Driven by esdACC-FD (Advanced CAN Core)

Basic Product Features:

- CAN ISO 11898-1 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Tests
  "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Bit rates from 10 kbit/s up to 8 Mbit/s supported
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Disable Automatic Retransmission (DAR)
  (Single-shot transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Self-reception mode (reception of 'own' messages)
- Busload measurement

Superior esdACC Features [1]:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
  - Easy to program
  - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
  - Timestamping complies with the CiA 603 specification
  - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
  - Providing the means to generate 100% busload even with non-realtime operating systems
  - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
  - High priority
  - 64-bit timestamp
  - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
  - e.g. for driver timeouts
  - ISO11898-1 conform
  - Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) [1]:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Optional integration with 32-bit microcontroller to further relieve host CPU
- CAN error injection units
  - Simulating a wide range of error situations on CAN bus, e.g.:
    - ID pollution (100% bus load on certain CAN ID/priority)
    - Defective sensor (Destroying all CAN messages of a given CAN ID)
  - Different trigger modes
    - Bit pattern match
    - Time triggered
    - Immediate regarding CAN arbitration
    - External
  - 'Cross CAN bus triggering'
    (event on one CAN bus triggers event on another bus)
- Optional different sources for timestamps (e.g. IRIG-B)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx® Spartan® and Intel® Cyclone® FPGAs.

[1] Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.

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