

CAN-PCIe/402

PCI Express® Board with up to 4 CAN CC or CAN FD Interfaces

Single Lane PCI Express Board with FPGA for up to 4x CAN CC or CAN FD

- 1, 2 or 4 CAN interfaces according to ISO 11898-2, up to 8 Mbit/s
- Bus mastering and local data management by FPGA (esdACC)
- PCIe® interface according to PCI Express Specification R1.1
- Selectable CAN termination on board
- Supports MSI (Message Signalled Interrupts)

Wide Range of Operating System Support and Advanced CAN Diagnostic

- Software drivers for Windows® and Linux® included free of charge
- Optional CAN layer 2 software drivers for real-time operating systems
- CANopen®, J1939 and ARINC 825 protocol libraries are available
- ISO 16845:2004 certified esd Advanced CAN Core (esdACC)
- High resolution hardware timestamps

Variety of Product Designs

- 4x CAN via DSUB37 connector
- Low profile version for 1x or 2x CAN
- Version with SIC transceivers

Wide Choice of Hardware Designs

The CAN-PCIe/402 is a PC board designed for the PCIe bus that features one, two or four electrically isolated CAN Classic (CAN CC) or CAN FD interfaces according to ISO 11898-2.

CAN-PCIe/402-4/2Slot features 4 CAN CC interfaces as a bundle of the 2 CAN CC version CAN-PCIe/402-2 and the extension adapter CAN-PCIe/402-Slot2.

CAN-PCIe/402-B4 is the versions with all four CAN interfaces equipped on a single board. They can be connected via one DSUB37 connector in the front panel.

CAN-PCIe/402-1-LP is the low-profile version and can be extended by a second CAN interface using the adapter CAN-PCIe/402-1-LP2.

CAN-PCIe/402-2-FD-SIC features 2 CAN interfaces with CAN signal improvement capability by usage of SIC transceivers.

CAN Data Management

The independent ISO 11898-1 conform CAN nets are driven by the esdACC (esd Advanced CAN Core) implemented in the

FPGA.

The esdACC supports bus mastering (first-party DMA) to transfer data to the host memory. This results in a reduction of overall latency on servicing I/O transactions especially at higher data rates and a reduced host CPU load. Due to the usage of MSI (Message Signalled Interrupts) the CAN-PCIe/402 can be operated in Hypervisor environments, for example. The CAN-PCIe/402 provides high resolution hardware timestamps.

Software Support

Windows and Linux (NTCAN-API)

The CAN layer 2 drivers for Windows and Linux are included in the scope of delivery.

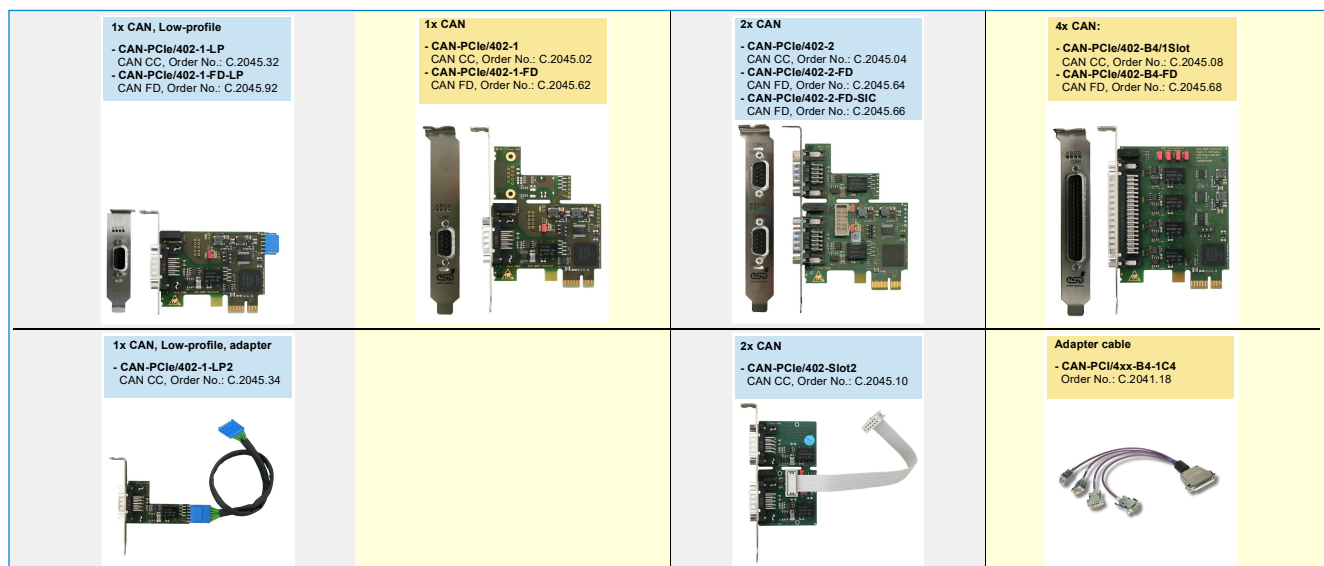
Real-time OS (NTCAN-API)

CAN layer 2 drivers for QNX® RTX® and RTX64® and VxWorks® can be ordered separately. Others are available on request.

Higher Layer Protocols (CAN CC only)

Higher Layer Protocols are available for many operating systems.

- CANopen Master- and Slave-Stack
- J1939
- ARINC825



Technical Specifications:

PCI Express Interface:	
PCIe port	PCI Express Spec. R1.1, Link width 1x
CAN:	
Interface	1x, 2x or 4x CAN interfaces with electrical isolation, according to ISO 11898-2, bit rates up to 8 Mbit/s
CAN controller	esdACC in EP4CGX FPGA, acc. to ISO 11898-1 (CAN 2.0 A/B)
General:	
Power supply	3.3 V: 2x CAN I_{MAX} = 280 mA, 4x CAN I_{MAX} = 290 mA 12 V: 2x CAN I_{MAX} = 180 mA, 4x CAN I_{MAX} = 230 mA
Ambient temp.	0 °C ... +75 °C
Rel. humidity	Max. 90 % (non-condensing)
Connector	PCIe: PCIe card edge connector CAN: 1x DSUB9 per CAN channel (all except C.2045.08), pin contacts 1x DSUB37 (C.2045.08 only), pin contacts
Weight	CAN-PCIe/402-2: 60 g

Order Information:

Hardware	Order No.
CAN-PCIe/402-1	1x CAN CC via DSUB9 C.2045.02
CAN-PCIe/402-1-FD	1x CAN FD via DSUB9 C.2045.62
CAN-PCIe/402-2	2x CAN CC via DSUB9 C.2045.04
CAN-PCIe/402-2-FD	2x CAN FD via DSUB9 C.2045.64
CAN-PCIe/402-2-FD-SIC	2x CAN FD, DSUB9, SIC-Transceiver C.2045.66
CAN-PCIe/402-4/2Slot	4x CAN CC (C.2045.04, C.2045.10) C.2045.06
CAN-PCIe/402-B4/1Slot	4x CAN CC via DSUB37 connector C.2045.08
CAN-PCIe/402-B4-FD	4x CAN FD via DSUB37 connector C.2045.68
CAN-PCIe/402-1-LP	Low-profile format, 1x CAN CC C.2045.32
CAN-PCIe/402-1-FD-LP	Low-profile format, 1x CAN FD C.2045.92

Accessories

CAN-PCIe/402-Slot2	Adapter, 2x CAN via DSUB9, cable	C.2045.10
CAN-PCIe/402-1-LP2	Adapter, 1x CAN CC/FD, DSUB9	C.2045.34
CAN-PCI/4XX-B4-1C4	Adapter cable DSUB37 to 4x DSUB9	C.2041.18

Software Support³

CAN layer 2 drivers for Windows/Linux are included in delivery free of charge. CAN layer 2 drivers for QNX®, RTX®, INtime and RTX64® and VxWorks® can be ordered separately.

³ For detailed information about driver availability for your operating system please contact our sales team.

CAN-PCIe/402

Driven by esdACC (Advanced CAN Core)



Basic Product Features:

- CAN ISO 11898-1:2015 protocol compatibility
- Tested and certified acc. to ISO CAN Conformance Tests "ISO 16845:2004 Road vehicles - Controller area network (CAN) - Conformance test plan"
- 11-bit and 29-bit CAN IDs
- Supported bit rates:
CAN CC: CAN classic also known as CAN 2.0A/B supports bit rates from 10 kbit/s to 1 Mbit/s with a payload of up to 8 bytes per frame.
CAN FD: CAN flexible data rate, supports bit rates from 10 kbit/s up to 8 Mbit/s with bit rate switch as well as a payload of up to 64 bytes per frame. It is fully backward compatible with CAN CC.
- Receive buffer (64 CAN messages)
- Complete access to CAN error counters
- Programmable error warning limit
- Error code capture register
- Error interrupt for each CAN bus error
- Arbitration lost interrupt with detailed bit position
- Disable Automatic Retransmission (DAR) (Single-shot transmission)
- Listen only mode (no acknowledge, no active error flags)
- Automatic bit rate detection (hardware supported bit rate detection)
- Self-reception mode (reception of 'own' messages)
- Busload measurement



Superior esdACC Features ¹:

- Operating system independently programmable via esd's NTCAN-API
- 32-bit register interface optimized for CAN needs
 - Easy to program
 - Transmission and reception of CAN frames with a minimum of register accesses
- RX and TX timestamping (64-bit wide, bit accurate, resolution may vary with input clock, in any case ≤ 62.5 ns, usually 12.5 ns)
 - Timestamping complies with the CiA 603 specification
 - On hardware with IRIG-B interfaces IRIG-B time is used for timestamping
- TX FIFO (16 CAN frames deep)
 - Providing the means to generate 100% busload even with non-real-time operating systems
 - Providing the means for real back-to-back transmission
- Timestamped Tx FIFO (16 CAN frames deep)
 - High priority
 - 64-bit timestamp
 - Bit time accuracy for CAN transmission
- Frame accurate abortion of transmissions with minimum delay
 - e.g., for driver timeouts
 - ISO11898-1:2015 conform
 - Aborted frames in FIFO won't be blocked by low priority TX

Superior esdACC Features (continued) ¹:

- Hardware timer to provide accurate software timeouts beyond operating system accuracy
- Bus mastering in RX direction takes the load off host CPU (needs bus master capable local bus to host interface)
- Using FPGA technology provides the option to tailor any feature to any customer's needs, including optional integration with customer's FPGA content
- The esdACC IP core has been verified on Xilinx® Spartan® and Intel® Cyclone® FPGAs.

¹ Availability of the Superior esdACC Features depends on the operating system. Please contact our sales team for further information.

For further information on the esdACC IP Core please contact our sales team.